Memrisys 2024

-Invited Speaker Session-

** Orange-colored invited speakers' abstracts will be updated soon.*

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Alon Ascoli	A Three-Element Second-Order Locally-Active Neuristor Reproducing the Cascade of Bifurcations, Underlying the Life Cycle of an Action Potential, in the Fourth-Order Hodgkin-Huxley Neuron Model
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Hiroyuki Akinaga	Reliability of ReRAM Device Technologies for Neuromorphic Applications

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Joon-Kyu Han	Next-Generation Computing Using Threshold Switching in Floating Body Transistors
Joshua Yang	Analog computing with high precision and programmability enabled by memristors
Juerg Leuthold	Photonic-Electronic Memristive Devices for Fast Neuronal Networks
Jung-Hae Choi	Ab initio study on charge transition-driven resistive switching in $Pt/TiO_2/Ti$ devices
Jung Ho Yoon	Oxide Nanostructure-based Memristor Research for Bio-inspired Computing Applications
Kazuya Terabe	Controlling ion transport at the atomic level to improve memristive devices
Keon Jae Lee	Simultaneous emulation of synaptic and intrinsic plasticity using a memristive synapse
Kyeong-Sik Min	Memristor crossbar circuits for low-power IoT devices
Kyusang Lee	Edge Intelligence towards Smart Sensing
Min Hyuk Park	Self-rectifying ferroelectric tunnel based on HfO2/ZrO2 superlattices

Ming Liu (Xumeng Zhang)	Neuromorphic Computing with Memristive Dynamics
Peng Lin	Modulation and application of ECRAM for Neuromorphic Computing
Qiangfei Xia	Tuning the dynamics of diffusive memristors for neuromorphic applications
Ronald Tetzlaff	Hybrid computing in memristive arrays
Sabina Spiga	Understanding the fundamentals of volatile memristors for brain inspired computing
Sangbum Kim	Neuromorphic Hardware with Phase Change Memory : Exploring Applications of Spiking Boltzmann Machines
Seyoung Kim	Analog AI Computation with Oxygen-Based ECRAM: Insights into Switching Mechanism and Cross-point Array Operations
Sreetosh Goswami	A 14-bit molecular dot product engine
Stephan Menzel	On the Relation between Switching Kinetics and Analog Programming Capabilities of Memristive Devices based on the Valence Change Mechanism
Su-In Yi	BackPropagation-free Deep Reinforcement Learning for Privacy-Preserving Recommendation system via Memristor crossbars
Suhas Kumar	Axon-like active signal transmission
Tae-Sik Yoon	Analog resistance changes in multilayer metal-oxide memristors for neuromorphic computing
Tamalika Banerjee	Memristive devices based on complex oxides as synapses and neurons
Themis Prodromakis	Linking real and artificial brains with memristor technologies
Thomas Dalgaty	Bayesian In memory computing with Memristors for adaptive intelligent machines
Toshiharu Saiki	Colloidal robotics using phase-change memory in individuals and the environment

Yoeri van de Burgt	Local and autonomous learning with organic neuromorphic electronics
Yuchao Yang	Large-Scale Memristor Integration for In-Memory Computing
Zhongrui Wang	Memristive computing : hardware-software co-optimization

Bio-Inspired Learning Rules on Opto-Electronic Memristive Hardware

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In traditional artificial neural networks (ANNs), each synaptic connection is represented by a single, static scalar value that updates only during training and remains fixed thereafter. In contrast, biological synapses exhibit complex dynamic behaviors, such as long-term plasticity, short-term dynamics, and meta-plasticity, all integrated within each synapse. This biophysical complexity is essential for the functioning of our nervous system and may explain the human brain's ability to interpret highly complex data in dynamic environments. Remarkably, this computational feat is achieved with ultra-low power consumption, roughly 20 watts. This contrasts with today's ANNs, which generally lack biological realism in their synapses and consume vast amounts of energy. The biological paradigm thus inspires the development of novel technologies that better capture the biophysical processes in synapses.

In this talk, I will introduce the fundamental devices of our opto-electronic memristive platform [1], which hold promise for enabling scalable and energy-efficient bio-inspired learning rules. I will first discuss the physics and switching mechanisms of our devices under light illumination through plasmonic/photonic circuits [2], Fig. 1(a). Then, I will show that light can provide an additional degree of freedom allowing for dynamic adjustment of the learning curve in two terminal memristive synaptic elements [3], Fig. 1(b). I will further show our latest hardware innovation: a single memristive device that replicates six synaptic operations observed in biological systems, using just two electrical terminals [4], Fig. 1(c). Lastly, an actor-critic network with analogue memristors that mimicks reward-based learning will be briefly discusssed [5].

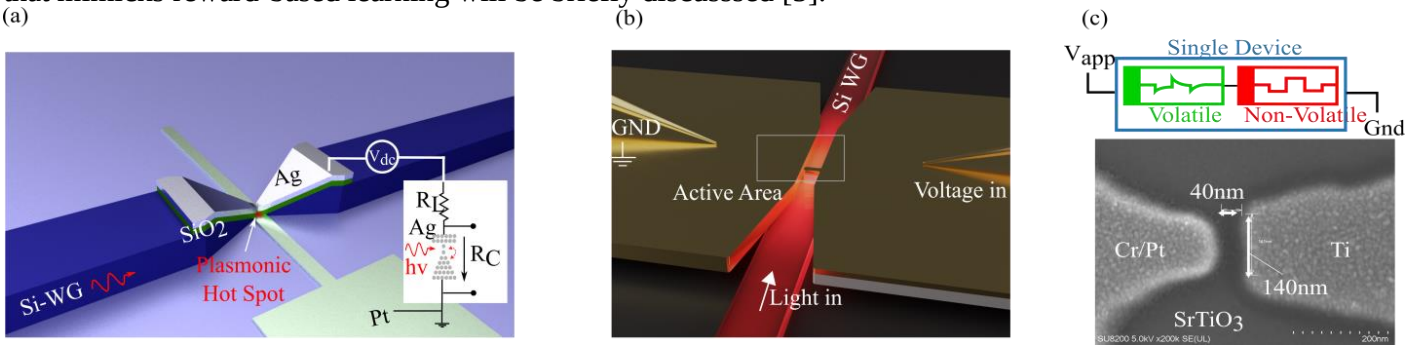

Fig. 1: (a) Schematic showing the concept of optical detection on Ag-SiO_2-Pt memristors (light-matter interaction). The plasmonic hot spot at the tip focuses energy on memristive junction and enables the reversible relocation of atoms between adjacent sites and thus the creation of two distinct electronic states. Light-matter interaction in memristive photodetector [2]; (b) Schematic illustration of a planar plasmonic Au-HfO_2-Ti/Au slot waveguide with a notch. An incident light signal in the silicon waveguide with an optical power is converted into a gap plasmon that subsequently heats the active area. This makes the filament broader due to heat-enhanced generation and diffusion of oxygen vacancies [3]; (c) Single neuromorphic memristor with multiple synaptic mechanisms [5]

Acknowledgement
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A Three-Element Second-Order Locally-Active Neuristor Reproducing the Cascade of Bifurcations, Underlying the Life Cycle of an Action Potential, in the Fourth-Order Hodgkin-Huxley Neuron Model

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A physical system, which is poised on a stable and locally active operating point, is said to be on the Edge of Chaos [1] therein. However, a system is endowed with a high degree of excitability under these circumstances. This explains why it may take just infinitesimal changes to the environmental conditions to push it away from the quiescent state, which typically results in the appearance of complex phenomena across the respective physical medium asymptotically. Recurring to the theoretical foundations of the Physics Principle of the Edge of Chaos, we recently explained the mechanisms underlying the emergence of symmetry-breaking effects, anticipating the steady-state formation of spatio-temporal patterns, in homogeneous reaction-diffusion neural networks from cellular biology [2]-[3], and from electrical engineering [4]-[5]. We have also invoked this universal Physics Law to elucidate the nature and origin of previously-unexplained oscillations in a neuronal cell [6], revealing the fundamental role of the Sodium ion channel for the emergence of the All-to-None phenomenon in biological axon membranes [7]. Most importantly, as discussed in this oral presentation, recurring to concepts from the Local Activity Principle and from Bifurcation Theory we were able to identify suitable parameter sets for operating a three-element circuit as the simplest ever-reported Hodgkin-Huxley neuristor [8]. In particular, leveraging the negative differential resistance effects in a NbOx threshold switch, the proposed neuronal cell employs solely the interaction between two dynamical states to reproduce the three fundamental bifurcations [9], occurring in the higher-order Hodgkin-Huxley neuron model [10] (refer to Figure 1), within the life cycle of an Action Potential (refer to Figure 2).

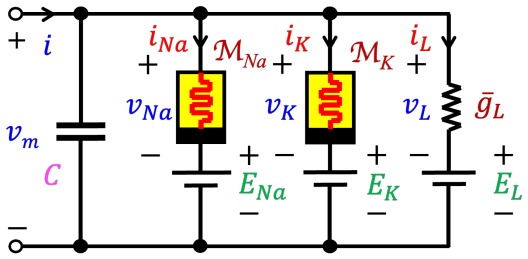

Figure 1. Equivalent Circuit of the Hodgkin-Huxley Neuron Model.

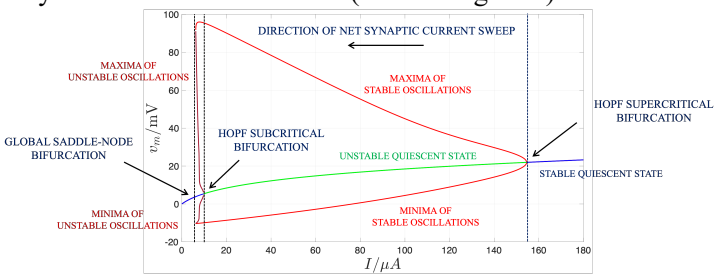

Figure 2. Bifurcation diagram of the Hodgkin-Huxley Neuron Model

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Analog PCM-based accelerator for large deep neural networks

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Deep neural networks (DNN) have been providing advancements such as in natural language processing, image processing and speech recognition. The DNN inferences are often utilizing graphic processing units (GPUs) and other DNN-specialized accelerators by taking an advantage of their parallelized multiply-accumulate (MAC) units since the MAC operations dominate arithmetic operations required in DNN algorithms. Since increasing the number of the model parameters tends to gain better inference performances as in recent evolution of Large Language Models [1], power consumption of the accelerators and their memory subsystems are also increasing according as the growth of model sizes. Therefore, building energy-efficient DNN accelerators is indispensable for further performance enhancements in AI applications using larger parameters.

Analog Non-Volatile Memory (NVM)-based in-memory computing concept was proposed for energy efficient DNN accelerators. In addition to its massively parallelized low-power analog MAC operations by using the NVM crossbar arrays, since the NVM arrays store model parameters and conduct the parallelized MAC operations using the parameters stored on the arrays, the architecture can mitigate Von Neumann bottleneck between processing units and memory subsystems, where conventional digital accelerators need to transfer parameters as well as input vectors [2].

While accuracy in each of the analog MAC arithmetic operation would not be exactly equivalent to accuracy in conventional CMOS-based digital floating-point operations, our 14-nm 35-million analog Phase Change Memory (PCM)-based in-memory computing chip achieved high energy efficiency and software-equivalent end-to-end inference performances in not only small but also large neural network models: RNN-Transducer in MLPerf [3, 4]. Then, we visit architecture studies to apply larger models.

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Quantum-inspired annealing in analog memristor crossbars for optimization problems

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Combinatorial optimization problems (COPs) are prevalent in social life and industry, with applications in computer science, engineering, chemistry, logistics, economics, and more. However, they are notoriously difficult to solve exactly. Analog computing in memristor hardware has shown potential for heuristic solutions, but current demonstrations are limited to series updates due to the constraints of simulated annealing and discrete-time Hopfield neural network models. In this talk, I will introduce our recent efforts in developing analog memristor hardware for efficient optimization problems. First, we propose borrowing concepts from quantum adiabatic annealing to the memristor-based Ising solver, achieving better parallelism by synchronously updating node states. We also adopt a binary neural network-inspired updating algorithm, experimentally demonstrating better efficiency and solution quality. Additionally, we developed a continuous-time version by employing the power minimization principle for natural energy gradient descent. By continuing to push the boundaries of analog computing, we hope to unlock new possibilities in optimization and contribute to advancements in various fields reliant on these complex problem-solving capabilities.

Analog Reservoir Computing Utilizing IGZO Channel Ferroelectric-gated Transistors

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Analog reservoir computing (In the landscape of contemporary computing, deep neural networks (DNNs) have gained prominence by enabling breakthroughs across various applications from image classification to healthcare technologies [1]. Although DNNs and their feedforward configurations have shown remarkable success in executing static tasks such as pattern recognition [2], they are unsuitable for processing dynamic data. In this context, recurrent neural networks (RNNs), specifically analog reservoir computing (ARC) systems, have emerged as pivotal solutions [3]. An ARC system employs a dynamic reservoir that projects the input data nonlinearly into a high-dimensional feature space. This mapping, facilitated by the intrinsic short-term memory capabilities of the reservoir, enables the transformation of complex inputs into linearly separable states within the system. The linearly weighted summation of these states is then processed using a trainable readout network, making ARC an efficient and robust framework for temporal data processing and prediction tasks. However, conventional ARC systems based on complementary metal-oxide-semiconductor (CMOS) platforms suffer from a deficiency in inherent dynamic response characteristics. This necessitates the use of complex algorithms along with large-scale integrated devices to handle nonlinear dynamic tasks, thus hindering the complete realization of the potential of ARC. To overcome this limitation, the exploration of hardware-based ARC systems utilizing novel materials and device configurations has garnered research interest; specifically, materials and devices that exhibit distinct volatile and nonvolatile switching characteristics to implement the reservoir and readout networks, respectively.

In this study, we introduce a fully integrated ARC system that exploits the material versatility of ferroelectric-to-morphotropic phase boundary (MPB) hafnium zirconium oxides, integrated onto indium–gallium–zinc oxide thin-film transistors (TFTs). MPB-based TFTs (MPBTFTs), which exhibit nonlinear short-term memory characteristics, are employed for physical reservoirs and artificial neurons (**Figure 1**), while nonvolatile ferroelectric TFTs simulate synaptic behavior for the readout networks (**Figure 2**).

Additionally, double-gate (DG) configurations of MPBTFTs enhance reservoir state differentiation and state expansion for the physical reservoir, processing both excitatory and inhibitory pulses for neuronal functionality as area- and energy-efficient leaky integrate-and-fire (LIF) neurons with minimal hardware requirements. The DG MPBTFT-based LIF neuron eliminates the need for capacitors and reset circuits by utilizing inherent partial polarization switching and volatile memory characteristics. The seamless integration of ARC components on a single wafer enables the execution of complex real-world time-series predictions with a low normalized root mean squared error. The material-device co-optimization proposed in this study paves the way for the development of area- and energy-efficient ARC systems.

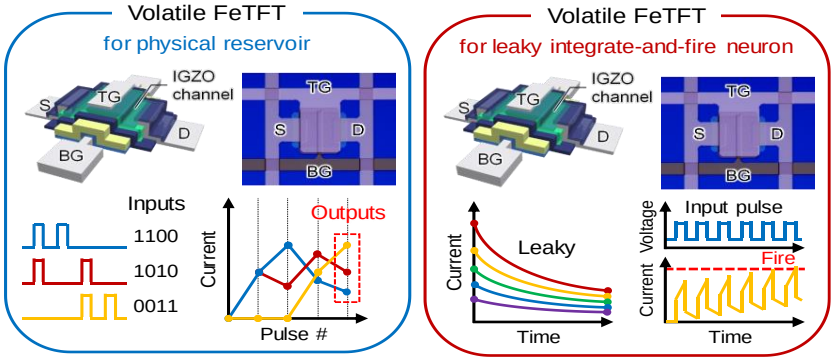

Figure 1. Physical reservoir and LIF neuron using MPBFET.

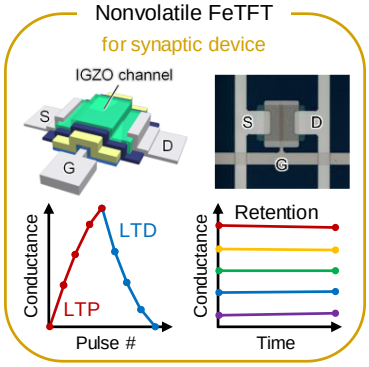

Figure 2. Synaptic behavior using FeFET.

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High-level computing-in-memory simulator

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Computing-in-memory (CIM) units combine random access memory (RAM) with processing elements (PEs) to execute various key linear algebra subprograms essential for deep neural network (DNN) operations. Distinguished from other deep learning (DL) accelerators such as neural processing units, CIM units function as RAM with substantial memory capacity. The on-chip memory capacity of DL accelerators is a crucial metric for large-scale DNNs, particularly for large language models. Consequently, CIM units with substantial memory capacity are garnering significant attention as a partial alternative to graphics processing units for the time being.

Among various CIM concepts, next-generation CIM units integrate memory and PEs into a single domain, enabling parallel multiply-accumulate (MAC) operations through analog operations like current summation or charge accumulation. These analog CIM concepts have been demonstrated using both volatile memories (e.g., static RAM (SRAM) and dynamic RAM (DRAM)) and nonvolatile memories (e.g., resistive RAM (RRAM), phase-change RAM, and magnetic RAM). Notably, SRAM and resistive RAM are widely adopted for analog CIM applications.

While several CIM simulators are available that simulate CIM operations at various levels, none consider CIM units embedded in the memory hierarchy. However, numerous simulators covering lower levels are accessible. To address this gap, we introduce a new CIM simulator capable of simulating the memory hierarchy (from DRAM to CIM tile with buffers in-between) for computing DNN models pre-trained using PyTorch. Key features include a fully reconfigurable memory hierarchy and buffer size (and tiles), with the simulator determining optimal buffering levels in terms of DRAM traffic.

At lower levels, key features include user-defined CIM memory type (SRAM or RRAM), MAC scheme (direct current read or charge accumulation), and operational parallelism (determining the resolution of analog-to-digital converters (ADCs) and the number of ADCs in use).

Title of the Presentation: Atomic Lego for future computing

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Short Biography:

Feng Miao joined Nanjing University as a full Professor of Physics and a Principal Investigator at Nanjing National Laboratory of Microstructures in July 2012. He received his Ph.D. degree in physics from the University of California, Riverside, United States, in 2009. Then he worked with HP Laboratories, Palo Alto, California, as a research associate for three years. He is a NSFC (National Science Fund of China) Distinguished Young Scholar, and the Chief Scientist of a National Key Basic Research Program. He has published over 130 technical papers (over 28000 citations, H index of 59, Web of Science) and is the inventor of over 30 issued/pending patents. His awards include: Chinese Physical Society “Huang Kun” Award (2020-2021), IAAM Medal (International Association of Advanced Materials, Sweden) (2021), China "Leading Scientists, Engineers and Innovators" (2019), Clarivate Analytics "Highly Cited Researchers" (2018), China "Young and Middle-aged Leading Scientists, Engineers and Innovators" (awarded by ministry of science and technology, China) (2018), "Jiangsu Youth Stars of Science and Technology" (Jiangsu province government) (2018), etc. His research is currently focused on electronic transport of two-dimensional materials and their applications for nanoelectronics, including emerging memory, advanced optoelectronics and brain-inspired computing.

Abstract:

Van der Waals (vdW) heterostructures (“Atomic Lego”) are formed by stacking layers of different 2D materials and offer possibilities to design new atomic structures with rich physics and functions. In this talk, I will show how these Lego structures provide unprecedented opportunities to explore new physics and realize device applications in the field of future computing, including neuromorphic computing, retinomorphic computing and quantum simulation. I’ll first present various Lego-structure-based neuromorphic devices we demonstrated, including highly robust memristors based on a graphene/$MoS_{2-x}O_x$/graphene vdW heterostructure [1], 2D moiré synaptic transistors and 2D moiré ferroelectric devices based on graphene/hBN heterostructures [2-3]. These Lego-structures can also be exploited to realize retinomorphic computing devices, such as prototype reconfigurable neural network vision sensor based on a WSe_2/BN heterostructure [4], and in-sensor broadband convolutional processing using a band-alignment-tunable $PdSe_2$/$MoTe_2$ heterostructure [5]. I will finalize my talk by discussing our preliminary explorations on new computing schemes based on these novel devices [7-8], and sharing our outlook for the future of this emerging field.

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Nonlinear Dynamics and Local Activity in Memristor Neuromorphic Circuits

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Nonlinear oscillators are systems which, undergoing very rich dynamics, are employable as primitives in several applications. Networks of oscillators exhibit complex interactions, which have been exploited in various works to address problems without efficient solutions on von-Neumann machines, including pattern recognition [1] and combinatorial problem optimization [2]. Under the fundamental principle of Local Activity, including its Crown Jewel, referred to as the Edge of Chaos, arrays of bio-inspired nonlinear oscillators, built with volatile memristors, may even process data similarly as biological systems [3]-[4].

Additionally, non-volatile memristive devices display nonlinear characteristics, which are particularly suitable to design circuits experiencing a plethora of complex dynamic behaviours, among which periodic oscillations and chaos, and transitioning between them via well-defined bifurcations. In a recent work [5], we presented the theoretical framework as well as the physical implementation of a memristive Chua's circuit, which leverages the programmable nonlinear conductance of a non-volatile ReRAM cell to switch between a number of different oscillatory operating modes through fundamental bifurcation phenomena.

All in all, the application of rigorous nonlinear circuit- and system-theoretic techniques [6], including the universal principle of Local Activity, allows to design bio-inspired neural networks, including reservoir computing systems, which exploit the unique physical properties of volatile and non-volatile memristors to outperform state-of-the-art computing machines [7].

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Mycelium-Based Engineered Living Materials Coupled with Memristive Networks: A Promising Emerging Future

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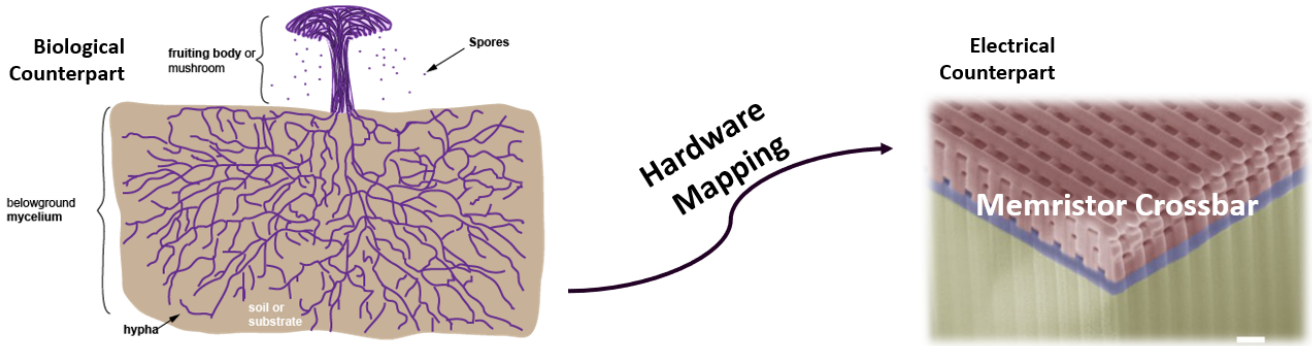
Engineered Living Materials (ELMs), particularly those based on fungal mycelium, represent a novel class of materials inspired by living organisms. These mycelium-based ELMs offer a sustainable solution to the escalating societal challenges posed by human-induced environmental disruption, resource scarcity, and increasing material demands. They are distinguished by their low-cost manufacturing process, natural ubiquity, and significant environmental advantages, including biodegradability [1]. However, due to the complex biological mechanisms they encompass, their environmental sensitivity, the slow supply chain and regulations, these materials present significant challenges for reproduction. For the researchers and engineers to accurately predict growth patterns, optimize conditions for mycelial ELM development, and assess potential applications, a digital twin would be advantageous. Digital twins, particularly those integrating novel electrical circuitry, emerge as an optimal solution. This is due to their inherent physical and mathematical intricacies, which enable a more profound comprehension of the underlying mechanisms of the models they represent.

Memristors, with their unique ability to both process and store information in a single component, are highly suitable for use in digital twins, particularly in the context of modeling Engineered Living Materials (ELMs), as can be observed in Figure 1. This suitability stems from their capacity to mimic the adaptive and evolutionary characteristics of biological systems. Specific analog hardware, including memristors, can be designed to emulate the electrical and morphological activities of ELMs. Memristors offer non-volatile memory, enabling them to maintain a state even when power is off, which mirrors the persistent nature of biological processes. Additionally, their ability to function at a low power consumption level, high density and their in-memory capabilities [2] make them ideal for continuously running systems like digital twins, which require consistent data processing and updating. For this purpose, the emphasis is placed on using memristive nanoelectronic circuits to simulate biological mycelium's hyphae evolution and electrical activity.



Crossbar Features	Biological Resemblance
2D-Grid Topology	Interscections of the latteral and vertical wires house memristor devices, creating an arrangement that propagates and processes electrical stimuli, providing the direct mapping of a mycelium network
Scalability	The crossbar topology is scalable, allowing for more dense and complex represenations of the mycelium's structure
Memristor Dynamics	RRAM's conductive fillament enables the modeling of the hyphae's rich dynamics
Sneak Path Current	Voltage drops across the array resemble the mycelium degradation and provide inherent branching by exploiting Ohm's Law
3D-Grid Topology	Crossbar structures can be vertically/horizontally stacked, enabling a one-to-one representation of the mycelium hyphae

Figure 1. Hardware representation of mycelium hyphae ELM with Suitability of memristive crossbars

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Neuromorphic Learning-in-Memory with Selector-less RRAM Crossbar Array

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To implement large-scale neuromorphic systems, a Resistive RAM (RRAM) crossbar array has become a key building block for high-density synaptic connections. Conventional RRAM-based AI accelerators use access transistors to mitigate cross-talks that can be induced by sneak paths and non-ideal factors. However, adding a selector on each memory cell limits the density of the array and increases the power consumption. Here, we present a reconfigurable hardware platform for parallel activation and programming of selector-less memristor-based crossbar arrays for AI training and interference applications. We proposed switched-capacitor voltage-sensing for read-out and Matrix-Vector-Multiplication (MVM) operations[1], which achieved lower power consumption and higher linearity than current sensing widely used for in-memory computing applications [2][3]. Moreover, the proposed read-out architecture can select the sensing time to characterize a wide range of resistances, which enables us to utilize our system as a benchmark platform for various selector-less crossbar types of memory devices. For the read-out scheme, we take the difference from both row and column, double-differential scheme, which enables us to achieve high read-out linearity and a large weight expression range. With the proposed sensing architecture, by utilizing Walsh-Hadamard encoded input vector, we demonstrate parallel conductance estimation with higher accuracy. The implemented system supports outer product-based online learning in memory with a parallel weight update technique, achieved through the four-phase decomposition of the weight matrix. Consequently, our system provides a user-configurable platform to accommodate a broad spectrum of RRAM device conductance measurements for synaptic crossbar arrays while supporting cognitive neuromorphic computing with online learning.

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A three-terminal vertical organic ferroelectric barristor for fast and energy-efficient neuromorphic computing

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In this presentation, I will introduce a three-terminal vertical organic ferroelectric barristor equipped with synaptic functions based on Schottky barrier height modulation to implement a neural network with parallel concurrent execution. The barristor can be extended to a diagonal neural network array while sustaining a crossbar array with nondestructive cell programming given the vertical stacking of layered gate line patterning on top. The array enables fast and energy-efficient operation of a diagonal convolutional neural network (CNN) that performs simultaneous weight update of cells sharing a kernel matrix. One-step convolution and pooling can be achieved, omitting sequential convolution for extracting and storing feature maps. The energy for vector–matrix multiplication on the MNIST and Clothes datasets using the diagonal CNN can be reduced by 75.80% and 71.79%, respectively, compared with the use of a conventional CNN structure while reducing the number of image sliding operations to one-fourth and achieving similar recognition accuracy of ~91.03%. Furthermore, I will present our most recent accomplishments, which include a 3D-stackable physical reservoir array and a finger recognition system, if time permits.

Keywords *: Neuromorphic Electronics, Three-terminal synaptic barristor, energy-efficient learning, Convolution Neural Network, MNIST*

Energy Intelligent Computing Devices Based on 2D Materials

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Abstract

Despite the long and crucial role of traditional solid-state physics for current silicon-based technologies, next generation neuromorphic, non-volatile memory, and energy devices that are key components in the era of the internet of things (IOT) require novel working principles with quantum physics emerging in low-dimensional materials[1-4]. The main research direction for the future devices is to realize 'ultralow device operation energy', 'ultrahigh device operation speed', and 'large-scale device integration (up to 10^{15})', which calls for exploring diverse quantum phenomena in low dimensional device components[5,6]. In this talk, I will present some of our recent efforts[1-7] to establish new device physics for energy intelligent devices, which could be a milestone for the promising future devices. In particular, dynamic convolution neural network, phase transition and other intriguing quantum physics in two-dimensional (2D) materials will be discussed along with logic device, neuromorphic computing, and energy device applications.

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Reliability of ReRAM Device Technologies for Neuromorphic Applications

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In MEMRISYS 2021, Natural Language Processing (NLP) was applied to the Review Papers to widely convey the knowledge to the readers of the conference proceedings [1, 2]. The knowledge graph generated from 8 Creative Commons licensed review papers published in the Proceedings of MEMRISYS 2021 showed that the top three terms in a device with a strong correlation with memristors were transistor, selector, and memory in descending order of weight. NLP with the Query in the order of Memrisor, Device to Challenges showed that the challenges analyzed as having the strongest correlation was endurance, followed by analog and multilevel conductance. In addition, the following terms were obtained when listed in descending order of weight; Beyond CMOS, Energy efficiency, Retention, Variability, Dynamic, von-Neumann bottleneck, Programmability, and Reliability. It may be said that the topic of reliability, which is extremely important for applications, was not yet the main subject of research and development at that time.

Resistive Random Access Memory, ReRAM, has been already introduced into the market, and research and development is actively being carried out for analog and memristive applications such as AI and neuromorphic applications. In this talk, we will discuss the resistance switching operation of ReRAM by theoretically examining the energy band structure, and then introduce our efforts regarding the reliability of ReRAM device operation. The first topics of the reliability is the evaluation of analog and multilevel-conductance behaviors assuming neuromorphic applications, which was pointed out in NLP described above. With reference to internationally standardized protocols, we investigated the origins of noise related to resistance variations in TaOx-based resistive switching memory [3]. The temperature dependence of the noise spectra at given frequencies revealed the existence of multiple trap levels, which were the origin of random telegraph noise and observed over a wide range of resistance values. The activation energies of the trap levels were clearly evaluated by the protocol. The second topics is the method to suppress the resistance drift, where “drift” means a phenomenon in which the average resistance value changes continuously with variations when switching is repeated, even under the same voltage application conditions. The possibility of accelerating drift mitigation by superimposing noise on the resistive switch process will be shown with the experimental results. We hope that these studies will promote applied research on memristors in a wide range of industrial fields.

Acknowledgements
A part of this study was performed together with Prof. Hiroshi Suga, Mr. Kota Sugawara and Mr. Kentaro Takaya. The theoretical research partially presented in this talk was conducted in collaboration with Prof. Kenji Shiraishi.

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Linearly programmable two-dimensional halide perovskite memristor arrays for neuromorphic computing

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Two-dimensional (2D) halide perovskites have emerged as promising artificial synapses because of their phase versatility, microstructural anisotropy in electrical and optoelectronic properties, and excellent moisture resistance. However, their asymmetrical and nonlinear conductance changes still limit the efficiency of training and accuracy of inference. Here, we achieve highly linear and symmetrical conductance changes (α_p: 0.002, α_d: -0.0015) in Dion-Jacobson 2D perovskites, which were unachievable previously in 2D perovskites [1]. We further build a crossbar array based on analog perovskite synapses experimentally for the first time, achieving a high (~100%) device yield, low variation (~1.85%) with synaptic weight storing capability, multilevel analog states with long retention (~10^4 s), and moisture stability over 7 months. We explore the potential of such devices in large-scale image inference via simulations and show an accuracy within 0.08% of the theoretical limit. The remarkable device performances are attributed to the homogenous migration of halide vacancies by eliminating gaps between inorganic layers, confirmed by first-principles calculations. Our materials design rule is generally applicable to other memristive material systems for achieving high-performance neuromorphic computing.

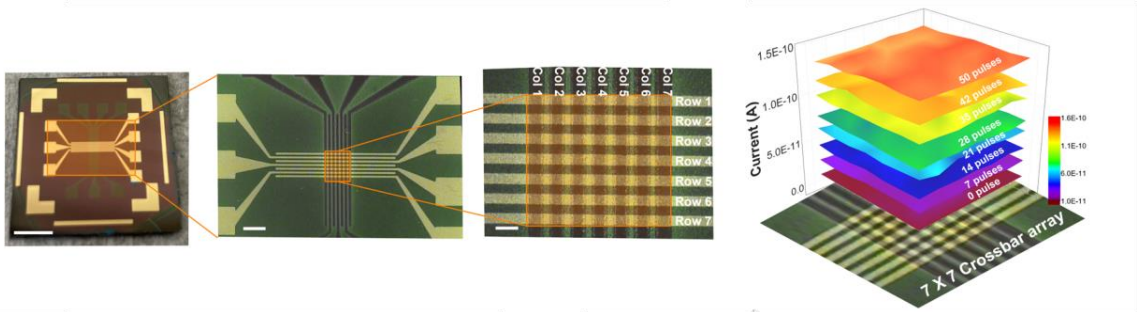

Figure. Optical images of 7 × 7 crossbar array with vertically aligned Dion-Jacobson perovskites artificial synapses. The scale bars indicate 5 mm, 1 mm, and 200 μm, respectively. A 3D mapping of 8 distinguishable analog states along with the synaptic pulses in a crossbar array is shown on the right.

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In-Memory Computing Applications with Memristor Crossbar Array

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Recently, there is a demand to develop efficient large-scale data processing methods with the advancements in artificial intelligence [1]. Conventional computing systems including von Neumann architecture, where the processing unit and memory unit are separate, are inefficient for processing large amounts of data. Therefore, in-memory computing is emerging as a promising solution because it can conduct computations within the memory unit, thereby enhancing computing efficiency [2]. The memristor crossbar array is one of the most widely used emerging memory devices to realize in-memory computing technologies [3]. Memristors offer several advantages, including a simple two-terminal structure, high cell density, and fast switching speed. In a crossbar array structure, vector matrix multiplication operations can be performed based on Ohm's law and Kirchhoff's current law, and various in-memory computing technologies including analog computing, stochastic computing, and digital computing can be realized. In this paper, we aim to introduce various in-memory computing technologies utilizing memristor crossbar arrays. First, we will introduce hardware artificial neural network structures with hardware tolerance through weight quantization [4]. By utilizing binary or ternary weight states, we can minimize performance degradation caused by device variations and discuss the learning methods for these neural networks. Additionally, we will present hardware security technologies that leverage randomness by semiconductor process variations. These include physical unclonable functions and true random number generators, which can be combined to create hardware security applications for generating unpredictable security keys [5, 6]. Finally, we will introduce digital logic operation techniques. When implementing threshold logic operations in memristor crossbar arrays, logical operations can be performed using read operations only, instead of switching operations [7].

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Hafnia-based Ferroelectric Transistors for Memory and Neuromorphic Device Applications

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Ferroelectric materials, characterized by their inherent ability to preserve polarization states without an external electric field, are set to significantly advance memory technology. Their unique property of polarization modulation via electric fields enables effective control over channel conductance, making them optimal for integration as gate dielectric layers in transistors. By integrating ferroelectric layers into transistors, it is possible to accurately regulate channel conductance, thereby improving the electrical characteristics of the device. Hafnia-based ferroelectrics are of particular interest due to their distinct advantages, such as compatibility with CMOS processes and processability. This innovative methodology provides a pathway for the fabrication of high-density memory devices. Ferroelectric transistors are emerging as a significant advancement in memory technology, providing high-density memory solutions and the potential to influence neuromorphic computing. This discussion investigates these promising prospects, proposing strategies to fully utilize the capabilities of ferroelectric materials in memory and computational applications. It further explores their potential to influence future memory technology. The distinct properties and potential applications of these materials make them a critical focus in the field of electronics and computing.

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Title: A Pathway to Large-Scale Neuromorphic Memristive Systems

Speaker: Jason Eshraghian

Abstract:
Memristors and neuromorphic computing go together like spaghetti and meatballs. Their promise of reaching brain-scale computational efficiency has significant implications for accelerating cognitive workloads, so why haven't we yet toppled NVIDIA from their throne? While consultants might say it's because of the lack of market inertia, and engineers might tell you there are still technical hurdles to overcome. This talk will focus on the technical challenges faced by circuit designers using memristors, specifically in the context of accelerating large-scale deep learning workloads. These challenges are well-established, and treated as design constraints in memristive circuits that presently exist. But overcoming those barriers remains an open question. This talk provides a guide on how we might overcome their challenges using systems-level approaches, and how spike-based computing could potentially be the right problem for memristive computing, ultimately pushing past what have historically been perceived as limitations.

Mixed Memristor-CMOS circuits for content addressable memories and in-memory computing

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Content Addressable Memories (CAM) offer a highly parallel pattern look-up capability, significantly enhancing many applications with a form of in-memory computing. However, capacities are limited in size and consume much power. We show that the use of non-volatile and analog memristive devices enable CAM circuits of higher data density and lower energy than CMOS-only counterparts. We further utilize such circuits in a variety of associative computing applications, including security, genomics, and machine learning. Going further, we are interested in how learning can be incorporated into such memory circuits and we describe a modified "differentiable" CAM circuit that is compatible with gradient-based training algorithms and illustrate some applications of such a circuit. We finally address challenges of these analog circuits, including the impact of temperature-sensitivity, CMOS process variations, and memristor read fluctuations.

Next-Generation Computing Using Threshold Switching in Floating Body Transistors

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A threshold switching property can be observed in floating body transistors, which is based on the single transistor latch (STL) phenomenon [1]. When a high voltage is applied, impact ionization occurs, causing excess holes to accumulate in the floating body and lower the potential barrier between the source and the body. This leads to more electrons being injected from the source to the body, generating additional holes and triggering a positive feedback loop. As a result, a catastrophic change is made, at which the current abruptly increases with a steep slope. Such threshold switching enables the floating body transistor to be applied to next-generation computing, which offers a significant advantage in terms of CMOS compatibility, allowing integration into the conventional CMOS ecosystem.

First, it can function as an artificial spiking neuron in neuromorphic computing [2,3]. Neuromorphic computing, which mimics the spatiotemporal processing of the brain using spike transmissions, has garnered significant interest for its superior energy efficiency. Artificial spiking neurons that generate spike signals are essential for this technology, and the floating body transistor can fulfill this role using threshold switching. Second, it can operate as a probabilistic bit (p-bit) [4]. Probabilistic computing leverages the principles and algorithms of quantum computing to solve complex combinatorial optimization problems more efficiently than conventional deterministic computing, without the need for cryogenic environments. P-bits, which generate probabilistic digital outputs, are crucial for probabilistic computing, and they can be implemented using the stochastic threshold switching in the floating body transistor. In this presentation, these applications of the floating body transistor in next-generation computing will be discussed.

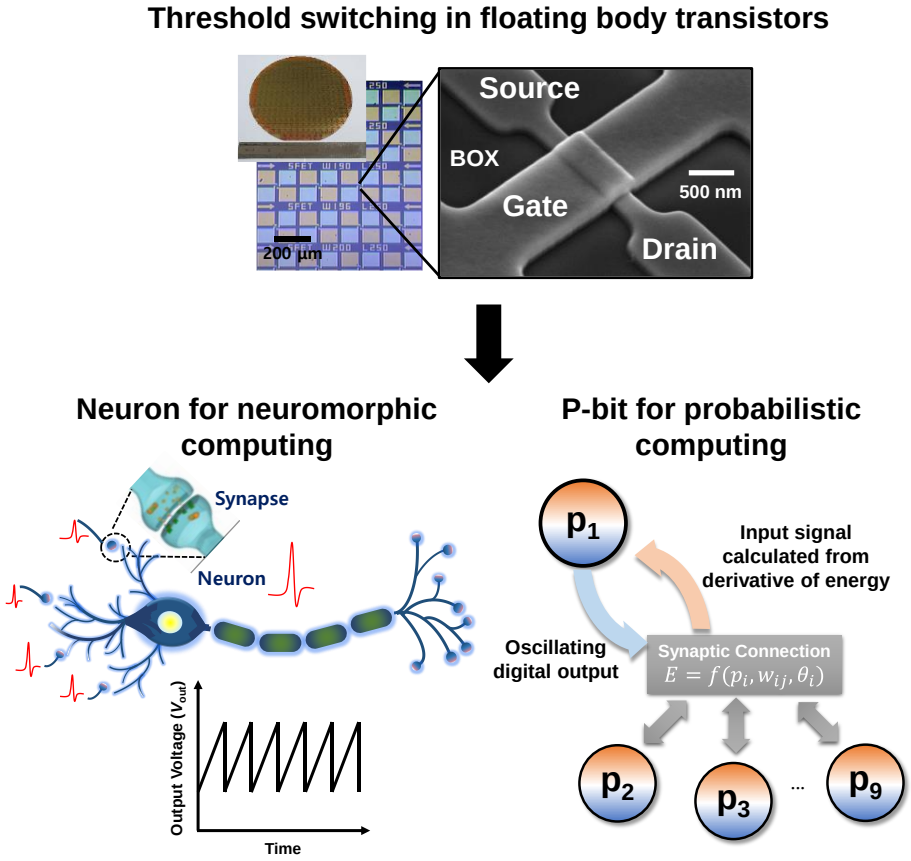

Figure 1. Threshold switching in floating body transistors and its application in neuromorphic computing and probabilistic computing

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Analog computing with high precision and programmability enabled by memristors

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While digital computing dominates the technological landscape, analog computing distinguishes itself with superior energy efficiency and high throughput. However, its historical limitation in precision and programmability has confined its application to specific and low-precision domains, notably in neural networks. The escalating challenge posed by the analog data deluge calls for versatile analog platforms. These platforms must not only exhibit exceptional efficiency but also sufficient reconfigurability and precision.

Recent breakthroughs in analog devices, such as memristors, have laid the groundwork for unparalleled analog computing capabilities. Leveraging the multifaceted role of memristors, we introduce memristive field-programmable analog arrays (FPAAs)[1], mirroring the functionality of their digital counterparts, field-programmable digital arrays (FPGAs). To elevate precision, we delve into the origins of reading noise, successfully mitigating it and achieving an unparalleled 2048 conductance levels in individual memristors—equivalent to 11 bits per cell, setting a record precision among diverse memory types[2]. Acknowledging the persistent demand for single or double precision in various applications, we propose and develop a circuit architecture and programming protocol[3]. This innovation enables analog memories to attain arbitrarily high precision with minimal circuit overhead. Our experimental validation involves a memristor System-on-Chip fabricated in a standard foundry, demonstrating significantly improved precision and power efficiency compared to traditional digital systems.

The co-design approach presented empowers low-precision analog devices to perform high-precision computing within a programmable platform. This demonstration underscores the transformative potential of analog computing, transcending historical limitations and ushering in a new era of precision and efficiency.

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Photonic-Electronic Memristive Devices for Fast Neuronal Networks

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A vison for a new generation of energy efficient electronic-photonic neural networks (NN) is discussed. It relies on previously introduced photonic-electronic memristive devices. The talk will discuss the physics and operation principles of the new elements. To demonstrate the potential of the technology, we will reconstruct a nonlinearly distorted 48 Gbit/s signal by classical DSP, by means of an electrical implementation of an artificial neural network (ANN) and by means of a photonic neural network (PNN). These neural networks will then be compared against the newly suggested NN.

Neural networks (NN) have been found to be powerful tools to handle artificial intelligence and machine learning problems. They are inspired by biological neural networks and as such rely on a layer of interconnected nodes, or neurons, which work together to transform input data into meaningful outputs. To build ANN and PNN one requires short and efficient electrical and optical on-chip interconnects as well as a multitude of volatile and non-volatile fundamental device building blocks.

In this talk we will introduce the concept of an electronic-photonic neural network. We will show that the fundamental building blocks for such a network such as a CMOS-compatible on-chip light source [1] (see Fig. 1), modulators [2, 3] (see Fig. 2) or photonic detectors [4] already exist. We will further show new elements such as volatile and non-volatile electrochemical metallization (ECM) memristors [5], or three-terminal memristors with a gate that allows to tune the set-voltage of the memristor [6] (see Fig. 3). Lastly, we show that memristors can be fast. We show operation of memristors in the 10s of picoseconds range [7] and elements switching with as little as a few mV [8].

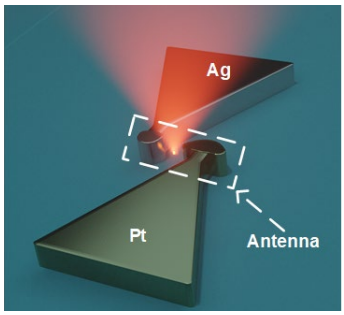

Figure 2. Memristive optical source: Cascades of photons are emitted upon operating the memristive element. See Ref. [1].

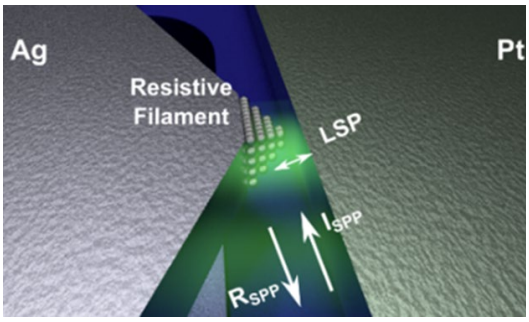

Figure 1. Memristive electrical and optical switch: When applying a voltage across the Ag-Pt electrodes, both electrical and optical switching is observed. More precisely, the optical surface plasmon polariton (SPP) will either pass or be reflected. See Ref. [3].

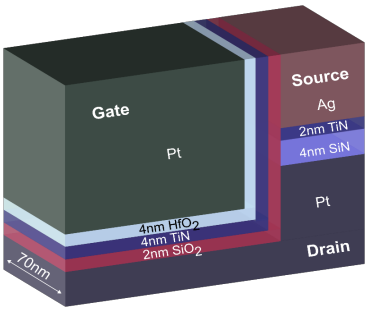

Figure 3. Three-terminal memristive cell allowing to control the set-voltage of the volatile electrical switch. See Ref. [6].

Ackhnowledgement

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Oxide Nanostructure-based Memristor Research for Bio-inspired Computing Applications

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Memristive devices have become a promising candidate for energy-efficient and high-throughput unconventional computing, which is a key enabler for artificial intelligent systems in the big data and IoT era. The so-called neuromorphic computing can be implemented on a resistive neural network with memristive synapses and neurons. In this talk, I will first briefly introduce oxide nanostructure-based memristive devices. I will then discuss the promises and challenges, including uniformity issues, non-linearity, and 3d structure compatibility, of the memristive devices & arrays, and also some approaches to overcome such issues.[1-6] A few examples selected from our recent experimental demonstrations of the promising applications from next-generation memory to bio-system emulator, which utilize such memristors, are also introduced.[7-9]

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Ab initio study on charge transition-driven resistive switching in Pt/TiO_2/Ti devices

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For valence-change type memory (VCM), redistribution of oxygen vacancies (V_Os) in conducting filament (CF) in response to applied bias is widely accepted as the major source of resistive switching. However, there is still controversy about the charge state of highly concentrated V_Os in the CF of thin film-based resistive random access memory (RRAM). The V_Os in the CF have been assumed to be positively charged (V_O^{2+}) to explain the field-driven switching of RRAM, but V_O^{2+} clusters in high concentration encounter Coulomb repulsion, rendering the CF unstable. Therefore, this study[1] investigates the oxidation state of V_Os in CF and their effects on the switching behavior via *ab initio* calculations using a Pt/TiO_2/Ti model system. The V_Os in the CF are in a low oxidation state but are transformed to (V_O^{2+}) immediately after release from the CF. The short-range interaction between V_Os facilitates the rupture and rejuvenation of the CF by reducing the corresponding activation energies. Finally, an improved switching model is proposed by considering the charge transition of V_Os. It provides a plausible explanation on the coexistence of two opposite bipolar switching polarities reported: the eight-wise and the counter-eight-wise polarities.

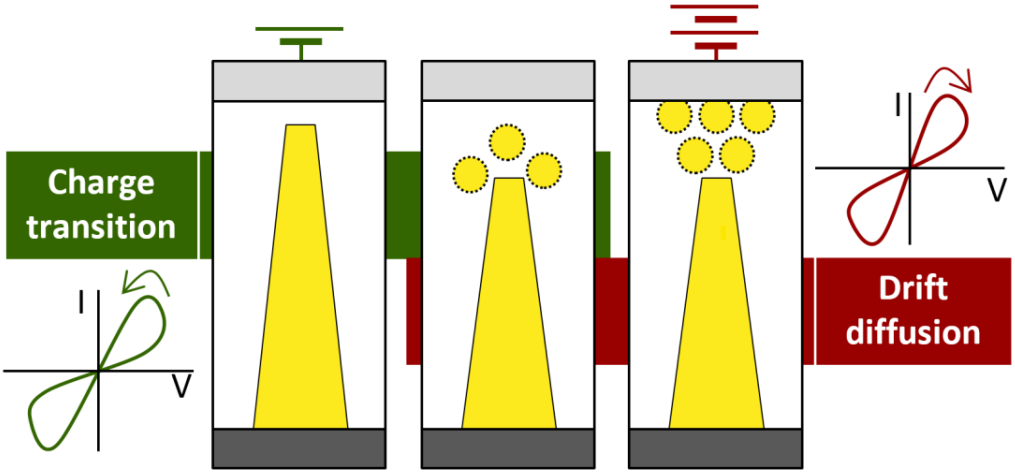

Figure 1. Schematics on the changes in the oxidation state of **V_Os** and their kinetics within CF and the relationship to RRAM switching behavior.

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Controlling ion transport at the atomic level to improve memristive devices

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It is well known that the properties and performance of functional materials used in various devices can be controlled by changing the arrangement and composition of the constituent atoms. The remarkable progress of nanotechnology in recent years has made it possible to control the ultra-fine structure and composition of semiconductor materials not only at the nanoscale but also at the atomic level, and these cutting-edge nanotechnologies have enabled the improvement of devices and circuits with superior performance and functionality at an ever-increasing pace. Compared with semiconductor devices, which operate by electron transport, memristive devices, which operate by ion transport as well as electron transport, have a shorter history of development research, and the development of functionality and performance by controlling them at the atomic scale has not been fully achieved. In this talk, we will introduce atomic-scale research on memristive devices to date (Figures 1 and 2), and discuss the importance of research and development using atomic-scale nanotechnology for the future device development [1-9].

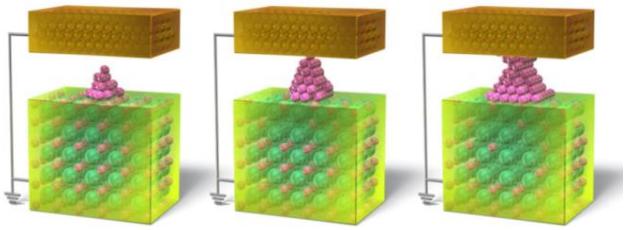

Figure 1. Memristive atomic switch that works by controlling a point contact at the atomic level using tunneling current [1].

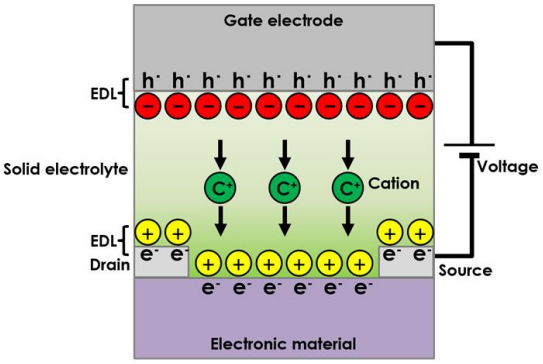

Figure 2. .Memristive all-solid-state transistor that works by controlling the electrical double layer (EDL) at the atomic level [9].

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Title: Simultaneous emulation of synaptic and intrinsic plasticity using a memristive synapse

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Abstract:

Neuromorphic computing targets the hardware embodiment of neural network, and device implementation of individual neuron and synapse has attracted considerable attention. The emulation of synaptic plasticity has shown promising results after the advent of memristors. However, neuronal intrinsic plasticity, which involves in learning process through interactions with synaptic plasticity, has been rarely demonstrated. Synaptic and intrinsic plasticity occur concomitantly in learning process, suggesting the need of the simultaneous implementation. Here, we report a neurosynaptic device that mimics synaptic and intrinsic plasticity concomitantly in a single cell. Threshold switch and phase change memory are merged in threshold switch-phase change memory device. Neuronal intrinsic plasticity is demonstrated based on bottom threshold switch layer, which resembles the modulation of firing frequency in biological neuron. Synaptic plasticity is also introduced through the nonvolatile switching of top phase change layer. Intrinsic and synaptic plasticity are simultaneously emulated in a single cell to establish the positive feedback between them. A positive feedback learning loop which mimics the retraining process in biological system is implemented in threshold switchphase change memory array for accelerated training. Our approach of bio-plausible mimicry can emulate biological working mechanisms to implement the complicated functional characteristics of a neural network for brain-like artificial intelligence.

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Keon Jae Lee received his Ph.D. in materials science and engineering (MSE) at the University of Illinois, Urbana-Champaign (UIUC) in 2006. Since 2009, he has been a professor in MSE at KAIST. His current research topics are self-powered flexible electronic systems including neuromorphic computing, flexible sensors, micro LEDs and laser material interaction.

Memristor crossbar circuits for low-power IoT devices

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Memristor crossbar circuits are a type of non-volatile memory that utilize memristors, passive circuit elements capable of simultaneously storing and processing data. The crossbar circuits has the capability to execute in-memory computing, hence minimizing the need for data transfer between the computing and memory units. By doing this, it leads to substantial energy saving in comparison to conventional von Neumann designs [1].

The Internet of Things (IoT) is a network that connects physical gadgets, automobiles, home appliances, and other goods. These products are equipped with sensors, software, and network connectivity, allowing them to collect large volumes of data from anywhere and exchange data among various IoT devices continuously. The Internet of Things (IoT) devices need to function using either battery power or energy-harvesting techniques, which requires the use of low-power designs.

On-device learning, often referred to as edge-learning, entails carrying out machine learning activities directly on the device, rather than depending on cloud-based computation. This method decreases the requirement for transmitting data to remote cloud computers, improving confidentiality and reducing the energy usage linked to wireless communication. On-device sensing refers to the process of incorporating different sensors, such as dynamic vision sensors, directly into the hardware of a device [2]. The sensors allow the device to collect information about its environment and carry out local data analysis, which reduces the requirement for constant data transfer between the edge and cloud computers and extends the battery's life time.

By integrating memristor crossbar circuits for efficient in-memory computing, Internet of Things (IoT) devices with on-device learning and on-device sensing capabilities, and optimized low-power designs, it is feasible to create energy-efficient systems that can function for long durations with restricted power sources. It is especially important for applications such as wearable devices, smart home automation, and remote monitoring systems, where power consumption is a vital factor. This presentation examines and explores the use of memristor crossbar circuits for the implementation of Internet of Things (IoT) devices capable of on-device learning and on-device sensing.

Acknowledgments

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Edge Intelligence towards Smart Sensing

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Recent advances in heterogeneous integration technology have made it possible to combine multiple functionalities on a single system. Among various, remote epitaxy techniques can produce single-crystalline membranes on graphene. We have recently discovered that “any types” of single-crystalline compound materials, such as III-V, III-N, and complex oxides, can be epitaxially grown on 2D materials-coated substrates. 2D material is sufficiently thin such that crystalline growth can be guided by the substrate beneath 2D materials. The slippery 2D surface allows the epitaxial films to be released from the substrate while the substrate can be reused. Based on this technology, various electronic and optoelectronic components can be fabricated and integrated. Integration of sensors and artificial neurons for artificial neural networks (ANNs) attracts great interest for the applications of artificial intelligence of things (AIoTs). Here, I will discuss how this advanced technology revolutionizes various sensors integrated with neuromorphic components for edge computing towards AIoTs.

Self-rectifying ferroelectric tunnel based on HfO_2/ZrO_2 superlattices

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Ferroelectricity in $(Hf,Zr)O_2$ based thin films have attracted increasing interest from both industry and academia since its first report in 2011.[1] Even in superlattices consisting of HfO_2 and ZrO_2, the ferroelectricity could be induced by engineering stacking order and relative thickness ratio.[2] The newly discovered fluorite-structured ferroelectrics have been suggested to be applicable ferroelectric memristor based on the tunneling conductance that can be modulated by the polarization states and resulting tunneling probability.[3,4] However, the memristive behavior of ferroelectric tunnel junction is not sufficient to justify its suitability to the neuromorphic computing applications with a simple crossbar array structure because of requirement of selector devices, insufficient on/off ratio, and poor linearity in potentiation and depression by identical pulses. In this presentation, a novel self-rectifying ferroelectric tunnel junction utilizing a $HfO_2/ZrO_2/HfO_2$ superlattice (HZH SL), in conjunction with Al_2O_3 and TiO_2 layers, is presented. The 6 nm-thick HZH SL effectively prevents the formation of non-ferroelectric phases while enhancing remnant polarization (P_r). This increased P_r adjusts the energy barrier configuration, resulting in a high on/off ratio of 1,273 by transitioning the conduction mechanism from thermal injection in the off-state to Fowler-Nordheim tunneling in the on-state. Additionally, asymmetric Schottky barriers at the top TiN/TiO_2 and bottom HfO_2/Pt interfaces provide a self-rectifying property with a rectifying ratio of 1,550. Simulations and calculations indicate that the device can support an integrated array size of over 7k, maintaining a 10% read margin and facilitating neuromorphic applications for artificial synapses with an image recognition accuracy exceeding 92%. The self-rectifying behavior and device reliability are validated in a 9 × 9 crossbar array structure.

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Neuromorphic Computing with Memristive Dynamics

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Neuromorphic computing draws inspiration from the information processing methods and architecture of the biological brain, driving technological innovation in the post-Moore era. Resistive switching devices, with their unique dynamic characteristics and diverse time scales, have emerged as ideal foundational components for constructing neuromorphic machines. This presentation will cover the core features of neuromorphic systems and the role of resistive switching dynamics within them. It will begin by discussing the critical role of short- and long-term synaptic processes in neuromorphic computing, along with our recent exploratory work in this area. The focus will then shift to neurons within neuromorphic systems, examining the importance of neuronal dynamics and presenting our recent advancements in highly biomimetic resistive switching neurons and their applications. Finally, the talk will conclude with a summary and outlook.

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Modulation and application of ECRAM for Neuromorphic Computing

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Utilizing rich properties in emerging nanoelectronic devices has offered new opportunities in designing more efficient hardware for a wide spectrum of artificial intelligence applications. By modulating the device composition, structure and fabrication conditions, the electrical behaviors of a device could be modulated such as enabling a transition from a non-volatile device to a volatile one. Here we explored the modulation and application of electrochemical memory (ECRAM) for neuromorphic computing. Firstly, a nonvolatile ECRAM was developed as artificial synapse with excellent linear potentiation and depression capabilities. A 10 x 10 prototype array was fabricated and suitable for on-chip learning tasks. Meanwhile, by adjusting the gate material of the ECRAM, we converted this non-volatile ECRAM into a volatile one. We observed controllable responses of this volatile ECRAM to pulse stimulations at various frequencies, enabling us to perform auditory sound classification using just a single device. Lastly, the ECRAM could be used in the neuron circuit design to modulate the behaviors of the neuron and contribute to four different firing patterns. The complex firing behavior could significantly enhance the processing capabilities of the spiking neural networks, thus providing new hardware solutions for more bio-plausible neuromorphic computing applications.

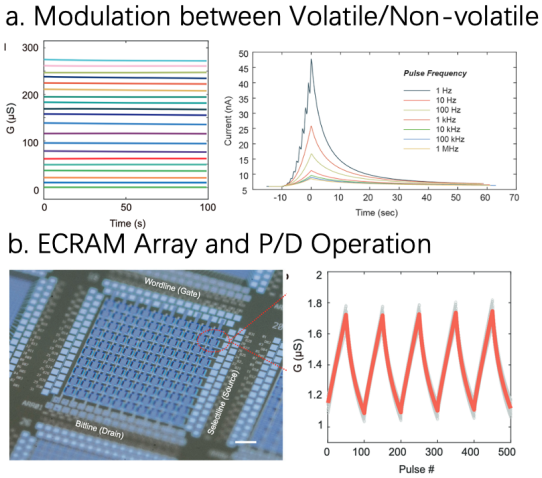

Figure 1: Modulation of ECRAM behaviors. a) a pair of ECRAM device with non-volatile and volatile behaviors. The volatile ECRAM shows controllable response to pulse stimulations at various frequencies. b) optical image of an ECRAM array, scalebar: 100 um, and repeated linear and symmetric conductance update of ECRAM.

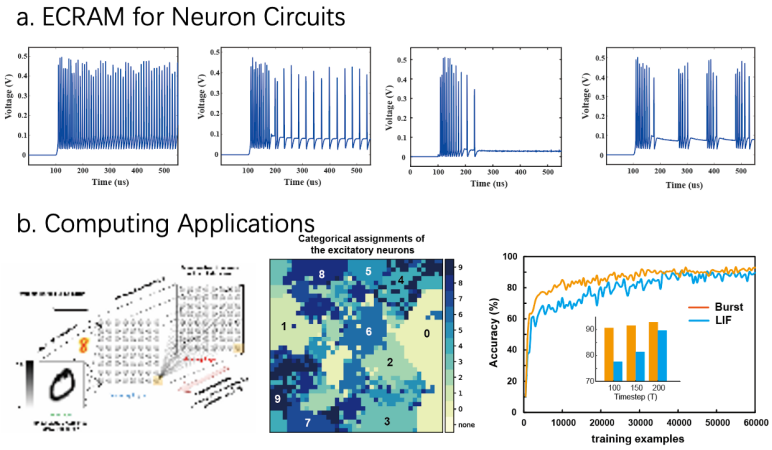

Figure 2: ECRAM for neuromorphic computing. a) ECRAM could be integrated into neuron circuits to modulate the behaviors of the neuron, four different firing patterns were observed by programming ECRAM. b) the rich dynamics in the neurons could be used for efficient neuromorphic computing applications, showing advantageous performance compared to a simplified LIF neuron.

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Tuning the dynamics of diffusive memristors for neuromorphic applications

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A diffusive memristor is a volatile resistance switch with a metal/oxide/metal structure. It goes to a low resistance state when an electrical stimulus is applied and automatically relaxes back to its original high resistance state if the stimulus is removed. The switching behavior is attributed to the formation and rupture of a localized conducting channel within the oxide layer. Because of their structural similarity with biological ion channels, diffusive memristors have been successfully used to emulate typical synaptic and neuronal behavior such as spike-timing-dependent plasticity, leaky integrate and fire, etc. However, a remaining issue of the diffusive memristor is the non-uniform and non-controllable relaxation time (the time it takes to go from low to high resistance states), which limits the wide-range adoption of such devices in large arrays for real-world problems. In this work, we designed and fabricated diffusive memristors with uniform and tunable relaxation times. We adopted a double oxide switch layer that led to an over ten-fold improvement in the cycle-to-cycle uniformity. By connecting the device to different resistors, we tuned the relaxation time up to three orders of magnitude. This controllable and uniform relaxation process was utilized to generate the time surfaces in the hierarchy of time surface (HOTS) algorithm for pattern recognition.

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Hybrid computing in memristive arrays

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While digital structures allow the implementation of mathematically precise computational methods, analog computations, in particular by exploiting phenomena of locally coupled nonlinear arrays, are extremely energy efficient and can be implemented on relatively simple cell structures. Within memristor-based computing architectures, where processing and data storage take place at the same physical location, locally coupled dynamic arrays have been proposed and theoretically studied in detail, showing a superior performance when applied as arrays of coupled oscillators or in pattern generating coding approaches. The emergence of complex behavior in such structures is based on local activity that must be poised at the edge of chaos, as is evident in some recent work on the design of multistable memristive arrays and with insights into the dynamics of neuron models. While each strategy has advantages for certain applications, a problem-specific combination of digital and analog methods becomes important when considering the latest approaches to in-memory computing.

Recent memristive analog computing methods are presented and discussed in detail. Based on M-Cellular Nonlinear Networks [1], hybrid structures are proposed that connect the analog domain with digital computing efficiently.

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Understanding the fundamentals of volatile memristors for brain inspired computing

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Innovative dynamical memristive devices are necessary for the realization of novel computing paradigms and to reproduce in hardware brain inspired computing primitives. Among the technologies under study, resistive switching electrochemical metallization (ECM) devices exhibit rich dynamical features thanks to their underlying physical mechanism. These devices can modify their resistance state in response to electrical stimuli such as voltage pulses, due to the formation (on state) and dissolution (off state) of nanoscale conductive filaments (CFs) formed by ionic migration from the electrode (usually Cu or Ag) through an insulating material. The CFs can be stable over several time scales (from ns to second, hours and even years) depending on the current compliance during programming and stack material composition, leading to the so named volatile and non-volatile resistive switching effects. In volatile ECM devices, the CF spontaneously dissolves once the electrical stimulus is released exhibiting a certain relaxation time. Due to these dynamical features, ECM devices have been proposed in literature as building blocks for both synaptic and neuronal implementations [1-2].

This work provides a comprehensive picture of the fundamentals at the basis of dynamical features of volatile memristors and how to exploit them for neuromorphic functionalities such as short-term plasticity, paired-pulse facilitation and inhibition observed in biological synapses, and integrative function of neurons.

A comprehensive characterization of prototypical electrochemical Ag/SiO_x/Pt memristive devices is performed by studying the device response to pulse stimuli (Figure 1,2) [3], unraveling how the interplay between switching times and relaxation effect controls the memristors dynamics and possible various switching modes. Further, we propose a comprehensive model to simulate the device operation and the evolution of the filament geometry under the effect of both surface diffusion and electromechanical stress, and mass injection due to electrodeposition of cations [4].

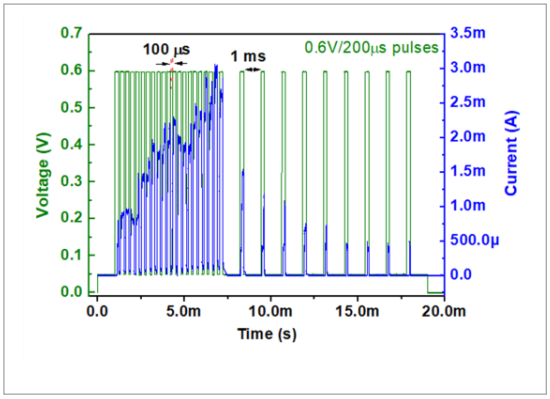

Figure 1. Example of relevant synaptic functionality implemented by the volatile memristive device, namely, pulse- pair facilitation and pulse- pair inhibition.

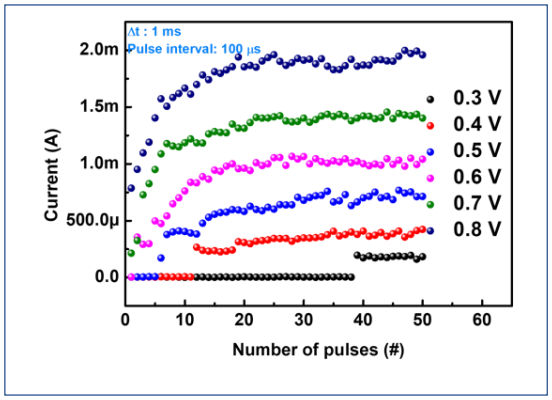

Figure 2. Representative device response to a train of 50 pulses showing integrative effects in the off state and cumulative switching in the on state as a function of pulse index and applied voltage.

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Analog AI Computation with Oxygen-Based ECRAM: Insights into Switching Mechanism and Cross-point Array Operations

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To meet the growing computational demands of artificial intelligence (AI) applications, there is a need for energy-efficient and high-performance computing architectures. Analog computing, particularly utilizing resistive cross-point arrays of non-volatile memory (NVM) devices, has emerged as a promising alternative [1, 2]. Electrochemical random-access memory (ECRAM) is a standout device technology candidate for such architectures due to its CMOS-compatibility, excellent programmability, and minimal variation across cycles and devices [3, 4]. Among the materials used, tungsten oxide (WO_{3-x}) offers large and continuous conductance tunability through ion migration, making it ideal channel material for analog switching ECRAM devices [5].

This study explores the key electrical properties of WO_{3-x} films through variable-temperature AC parallel dipole line (PDL) Hall measurements [6] on ECRAM devices with a multi-terminal Hall-bar structure [7, 8]. The AC Hall measurement system's high sensitivity to weak Hall signals from low-mobility and high-resistivity films like WO_{3-x} allows us to determine carrier mobility and density at various temperatures and conductance states [9]. These measurements provide valuable insights into the conductance switching mechanism of oxygen-based ECRAM devices. Furthermore, we discuss the implementation of large-scale ECRAM cross-point arrays and operational strategies to mitigate non-ideal device characteristics [10, 11], aiming to advance the development of energy-efficient and high-performance analog AI hardware [12].

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A 14-bit molecular dot product engine

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Molecular electronics have been a research topic for about three decades. The first wave in the nineties revolved around the appealing concept that molecules might make controllable nano-scale switches by self-assembly. However, the molecules proved to be fragile, and their switching endurance was far too low to be useful. Recently, molecular memristive circuit elements based on redox-active transition metal complexes of azo aromatic ligands have demonstrated resistive switching performance superior to inorganic oxides, which calls for a serious examination of their chemical and physical properties and potential applications. Beyond being a simple on-off switch or binary storage element, molecular memristors offer several unique features: deterministic (as opposed to stochastic) and uniform (as opposed to filamentary) resistance switching, multiple resistance levels, simultaneous memristance and memcapacitance, and multiple serial non-monotonic switching events. Can these characteristics offer a significant benefit to computing performance? In this presentation I shall talk about the potential advantages of molecular devices in the in-memory and neuromorphic computing. Starting from device fundamentals, we are currently looking into circuits and on-chip integration that could be promising platforms for artificial intelligence and machine learning in the post-Moore era.

I will highlight a recently developed 64 × 64 molecular crossbar [1,2], that enabled us to store information in 16,520 states per circuit element and achieve a 14-bit equivalent analog resolution (Fig. 1) [3]. A dot product engine made out of our molecular crossbar enables vector matrix multiplication (VMM) in a single time step. We conducted matrix multiplications involving various matrix-configurations, including symmetric, asymmetric, Hermitian, stochastic, and bi-stochastic matrices. Each computation resulted in >12-bit output resolution of the VMM product, which could cater to a wide range of scientific computing and artificial intelligence tasks. Utilizing the accuracy of our molecular crossbar, we could reconstruct space image from frequency domain data using inverse Fourier transform yielding a signal-to-noise ratio of 74dB. Additionally, by leveraging the high precision offered by our platform, we could perform both training and inferencing (forward and backpropagation) of an artificial neural network using our crossbar and achieved >90% accuracy in classifying MNIST (for handwritten digits) and EMNIST (for handwritten alphabets) data sets (Fig. 2). Training a neural network with a dot product engine had been an unattained goal in neuromorphic computing primarily limited by the low accuracy of the existing DPEs. Our platform has undergone rigorous testing by the Centre for Development of Advanced Computing (CDAC) and the Defence Research and Development Organisation (DRDO). It is currently being evaluated for field-integration into airborne self-navigating vehicles.

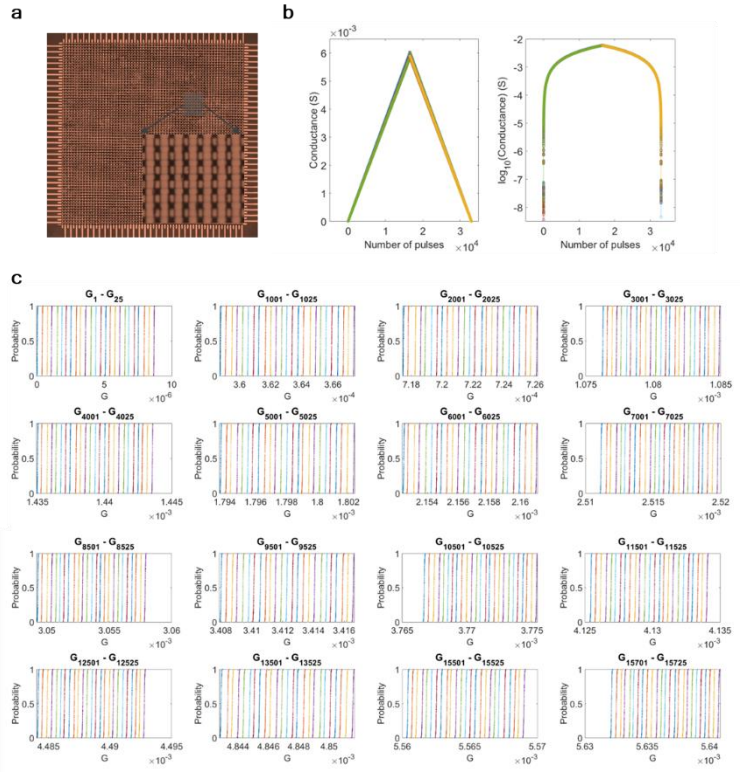

Figure 1: (a) SEM image of our Molecular crossbar platform. (b) The weight update curves from 4000 different cross points all showing linear, symmetric, 14 bit weight update characteristics. (c) Cumulative distribution of different representative conductance levels computed based on 2000 data points for each level.

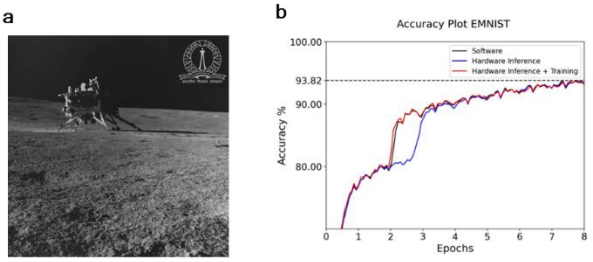

Figure 2: (a) Reconstructed image produced by the Indian Space Research Organisation from the frequency domain data using our crossbar. (b) The training accuracy obtained for training a neural network for EMNIST data set. We used our crossbar for performing VMMs for both training and inferencing.

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On the Relation between Switching Kinetics and Analog Programming Capabilities of Memristive Devices based on the Valence Change Mechanism

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Memristive devices based on the valence change mechanism (VCM) have attracted great attention for their use for non-volatile memory and neuromorphic computing applications. Their ability to be programmed to different resistance states enables performing analog vector-matrix multiplications (VMM) in memristive memory arrays in one shot. As VMMs are one of the main arithmetic operations required for neuromorphic computing loads, memristive devices promise energy-efficient neuromorphic computing hardware. To facilitate learning using backpropagation – as one of the most used learning paradigms – a highly linear update of the device's conductance on constant voltage pulses is highly desirable.

VCM devices can be realized using different combinations of insulating oxides in combination with metal electrodes. While the fundamental mechanism is based on the redistribution of ionic, typically oxygen, defects withing the oxide material, the electrical switching characteristics and dynamics can vary greatly. The most common type of VCM cells rely on the movement of oxygen vacancies in a nanoscale filament. The Joule heating produced during operation can lead to ultrafast switching and strongly non-linear switching kinetics but can also result in a thermal runaway which impedes the addressability of intermediate states by pulse trains.
In this talk, the impact of Joule heating on the transient behavior of memristive devices in dependence of filament size and series resistance is discussed theoretically. The theoretical predictions are compared with three different exemplary VCM systems [1]. Based on this, general guidelines to realize multilevel switching in VCM cells are developed by engineering the switching kinetics either by programming strategies or by material solutions. Experimental results and theoretical considerations suggest that analog switching can be achieved if a thermal runaway is avoided. Moreover, it will be shown that internal series resistances play a crucial role in controlling the runaway and determining the accessible resistance window. Finally, the interplay between a select transistor and the VCM cell is discussed during analog programming operation. It is shown that the programming characteristics differ depending on the connection of the VCM cell and the transistor and in which operation regime the transistor works [2].

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BackPropagation-free Deep Reinforcement Learning for Privacy-Preserving Recommendation system via Memristor crossbars

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Emerging recommendation systems leverage deep neural networks that can learn complex users' behavior, guiding them to compelling content. However, as data volumes grow, challenges arise in the time and energy efficiency of the backpropagation and extensive matrix-vector multiplication required for training and inference. Memristor crossbars, a form of brain-inspired hardware, offer a solution by combining synaptic and neuronal dynamics within an in-memory computing framework. Despite this, in-situ training without backpropagation has not yet been demonstrated. Here, we propose an algorithm for a backpropagation-free recommendation system, integrated into a deep reinforcement learning framework and implemented on large-scale memristor crossbar cores. Our approach introduces a hardware in-situ training framework and achieves balanced user selections in 4-user and 10-user scenarios, demonstrating effective recommendations and validating the scalability and flexibility of our system toward enhancing the total discounted reward. Compared to other artificial intelligence (AI)-computing systems, our hardware approach enables energy-efficient and fast computation, opening new avenues in AI, neuromorphic computing, and cybersecurity.

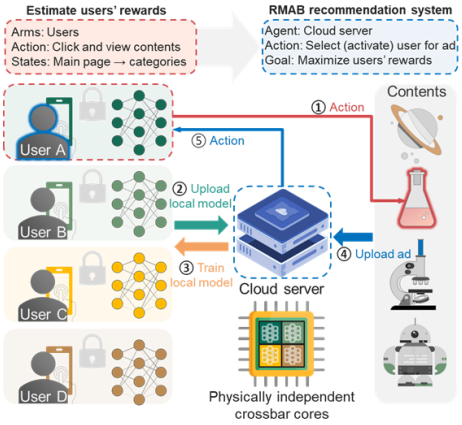

Figure 1. Schematic illustration of restless multi-armed bandit (RMAB)-based recommendation system through recovering bandit. Each arm (user-content pair) is trained independently, which preserves the privacy and resolves the curse of dimensionality common in multi-armed bandit (MAB) problems.

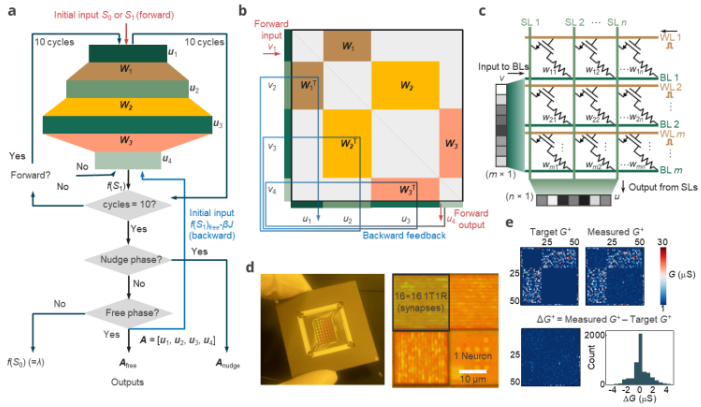

Figure 2. Hardware implementation of RMAB problem solver within deep reinforcement learning framework to infer the Whittle index of each arm. Activity-difference-based gradient calculations are performed instead of the backpropagation.

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Analog resistance changes in multilayer metal-oxide memristors for neuromorphic computing

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Conventional von Neumann computing systems face the challenges in limited advance in performance and heavy traffic issue in data transferring called von Neumann bottleneck in data-centric application [1]. As a solution to overcome the limitation in von Neumann systems, the brain-inspired neuromorphic computing attracts significant attention for its advantages of high energy efficiency in computation, superior processing capability for unstructured data, and so on [2]. In neuromorphic computing systems, the artificial synapse devices are essential elements for processing incoming input signals associated with stored synaptic weights as well as learning by updating the weight consequently. For these operations, the resistance changing memristors have been actively investigated as artificial synapses with various resistance changing materials and structures [3]. In these memristors, analog resistance changes are highly beneficial to processing and storing multilevel information effectively, which consequently enhances the computation performance and energy efficiency. In this talk, the characteristics of analog resistance changes in memristors using multilayer metal-oxides, for example, HfO_2/HfO_{2-x} [4], Gd-doped CeO_2/CeO_2 [5], $LiCoO_x$/NiO [6], and p-NiO/n-ZnO/p-NiO [7], are discussed for neuromorphic computing applications.

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Memristive devices based on complex oxides as synapses and neurons

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With the rapid rise of computing applications in Artificial Intelligence and Internet of Things, strategies for collocating memory and compute in a single device is actively pursued and is expected to alleviate the large power consumption in such computing hardware. At the hardware level, the present system lacks the rich non-linear phenomenon that occurs in biological systems and in this the rich phase space offered by complex oxides with correlated properties is an important platform. Intrinsic to these materials and their devices are emergent phenomena at their heterointerfaces which can be tailored by strain and doping and tuned by external stimuli such as temperature, electric field and magnetic field. This talk will discuss new examples of non-linear systems akin to synapses and neurons – components of any neuromorphic hardware made up of such materials. In the first part, I will discuss areal downscaling of interface memristive devices directly integrated on a semiconducting Nb-doped $SrTiO_3$ (Nb:STO) platform. We show surprising enhancement in the memristive memory window, while maintaining analog behavior, contrary to expectations. The device designs on such semiconductors allows leveraging electric field effects at edges, increasing the dynamic range in smaller devices with high endurance and low device and cycle variation down to the smallest devices with read out at low power. In the second part I will discuss how interfaces of thin manganite films on an oxide substrate exploit the octahedral orbital coupling effects and demonstrates anisotropic transport that persists over large length scales in a network. Electronic instabilities manifested as negative differential resistance (NDR), exploiting the intrinsic metal-to-insulator coupled transition are observed. Multiple NDR regimes at different voltage bias have been exploited to demonstrate voltage control oscillators with tunable frequencies and these have been harnessed to demonstrate leaky integrate and fire neurons in the entire architecture.

These devices lend well for data analysis tasks such as in classification, clustering and pattern recognition as used in neuromorphic computing applications.

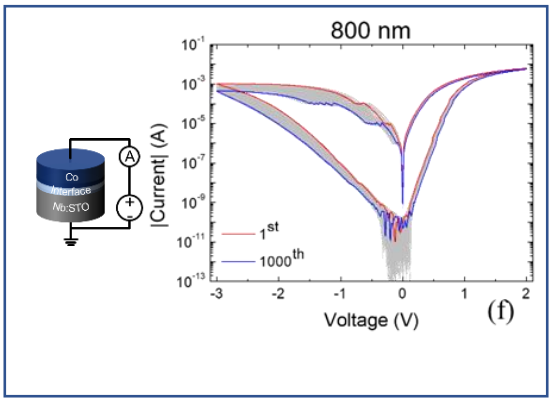

Figure 1. Interface memristive devices as synapses

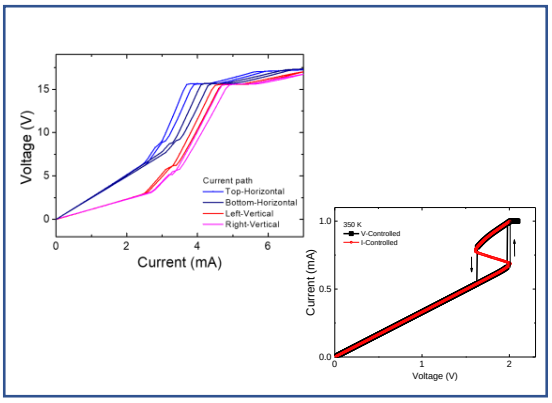

Figure 2. Anisotropic switching and hagative differential resistance in manganites

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Themis Prodromakis - University of Edinburgh

Linking real and artificial brains with memristor technologies

Never before has the merge between biology and engineering being so strong, with Implantable electronic systems enabling unprecedented applications in neural impairments and prosthetic control. For these solutions to be effective, the technologies used need to be biologically compatible while providing enhanced performance across: power consumption, detection accuracy, overall footprint, and latency. Previously, our group has demonstrated how the fundamental thresholded integration attribute of memristor devices can be utilised in detecting and classifying neuronal spikes in real-time, paving the way for a new neuroprosthetic technology that processes signals in similar ways to biological synapses. Here, we expand this work by demonstrating a memristor-based processing system for single-trial detection of behaviorally meaningful brain signals within a timeframe that supports real-time closed-loop intervention. We record neural activity from the reward center of the brain, the ventral tegmental area, in rats trained to associate a musical tone with a reward, and we use the memristors built-in thresholding properties to detect nontrivial biomarkers in local field potentials. This approach yields consistent and accurate detection of biomarkers >98% while maintaining power consumption as low as 4.14 nanowatt per channel. The efficacy of our system's capabilities to process real-time in vivo neural data paves the way for low-power chronic neural activity monitoring and biomedical implants.

Bayesian In-memory computing with Memristors for adaptive intelligent machines

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CEA Grenoble, France

Memristors are a key technology to enable low-energy and low-latency in-memory computing for future AI systems. However, the cycle-to-cycle and device-to-device variability of Memristors has largely limited their application domain to low-precision neural network inference. In contrast, the intelligent machines of the future will be required to adapt themselves continually as their environment and objectives change. The Bayesian framework permits this limitation to be turned into an advantage, where Memristors may be considered instead to be very high-precision physical random variables as well as memory elements. This provides a pragmatic path towards realising the adaptive in-memory computing systems of the future. We review our recent work that uses Memristors to accelerate two Bayesian machine learning approaches – variational inference [1,2] and Markov chain Monte Carlo (MCMC) [3,4] (Fig.1). We conclude with some recent results and perspectives on the future of this promising new approach.

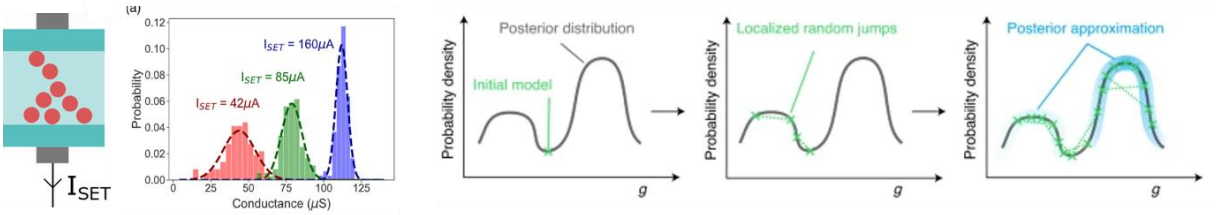

*Figure 1 – **The principle of Memristor-based Bayesian computing**. (a) Measurements of the conductance probability distributions when programming a Memristor with three different currents one thousand times. The current conditions the distribution of the Memristor random variable. (b) Memristor variability can be exploited to implement Bayesian algorithms. Here, an MCMC algorithm is illustrated which permits samples to be drawn from complex probability distributions of parameters, often neural network weights.*

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Colloidal robotics using phase-change memory in individuals and the environment

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The collective behavior of organisms involves some optimization from the point of view of time, energy, and risk management. There have been studies to interpret and algorithmize their behavior using mathematical models and to use them as a solution search method for optimization problems. However, the current state of mathematical models is far from understanding the essence of biological behavior. For example, it is difficult to model the role of memory and internal states of behavioral history based on biological observation alone. It would be useful to conduct research using a real physical system that can introduce various interaction mechanisms while simulating living organisms. In this study, we aim to construct a real physical system in which colloidal particles are considered as individual organisms, and the interaction with the environment and the history of interactions between individuals are stored by phase-change materials to manifest purposive behaviors.

Colloidal particles of 3 μm diameter moving in water were used as ants to implement a pheromone communication mechanism using a phase-change material and photothermal lens effects [1]. The keys to the implementation are (1) the self-propulsion ability of the particles, (2) the pheromone attraction ability, and (3) the controllability of the relative ratio of these two abilities. Self-propulsion is achieved by using Janus particles (hemispherical surface of polystyrene particles coated with gold), which are propelled under an alternating electric field. The pheromone-attracting ability is realized by using a chalcogenide phase-change material (GeSbTe) as a substrate (the ground on which the ants move). When a wide area subnanosecond pulse of light is applied from above, the GeSbTe is heated by the lens focusing effect directly below the particle and changes from an amorphous phase to a crystalline phase. Since the crystallization occurs along the trajectory of the Janus particles, it is considered a pheromone emission. Furthermore, the local formation of a highly conductive crystalline phase causes the AC electric field to be concentrated in the crystalline phase region, which eventually generates an electro-osmotic flow. Since this flow is always directed toward the crystalline phase region, it can be used as a pheromone attraction. Although both particle self-propulsion and pheromone attraction originate from the AC electric field, their relative proportions can be controlled depending on the frequency. When the pheromone attraction ability is enhanced, self-trapping occurs and bacterial colonization can be mimicked. GeSbTe can also be used as a coating material for the particles themselves to implement memory functionality. Between the two phases it is possible to switch the self-propulsion velocity and the inter-particle interaction [2].

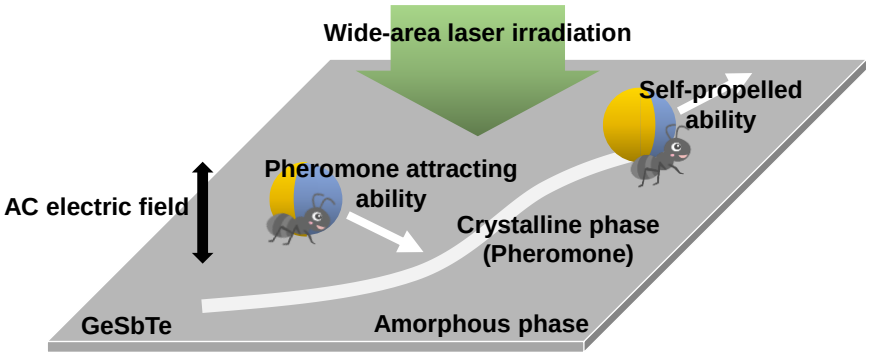

Figure 1. Implementation of pheromone communication mechanism by using a phase-change material and photothermal lens effect.

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Yoeri van de Burgt – Eindhoven University of Technology

Local and autonomous learning with organic neuromorphic electronics

Neuromorphic engineering takes inspiration from the efficiency of the brain and focusses on how to utilise its functionality in hardware. Organic electronic materials have shown promising solutions for the manipulation and the processing of biological signals, with applications ranging from bioinformatics to brain-computer-interfaces and smart robotics.

This talk describes state-of-the-art organic neuromorphic devices and provides an overview of the current challenges in the field and attempts to address them. I demonstrate a device concept based on novel organic mixed-ionic electronic materials and show how we can use these devices in trainable biosensors and smart autonomous robotics. I will present a novel implementation of backpropagation with gradient descent directly in hardware.

Next to that, organic electronic materials have the potential to operate at the interface with biology. This can pave the way for novel architectures with bio-inspired features, offering promising solutions for the manipulation and the processing of biological signals and potential applications ranging from brain-computer-interfaces to bioinformatics and neurotransmitter-mediated adaptive sensing. I will highlight our recent efforts for such hybrid biological memory devices and artificial neurons.

Large-Scale Memristor Integration for In-Memory Computing

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As Moore's law slows down and memory-intensive tasks get prevalent, digital computing becomes increasingly capacity- and power-limited. In order to meet the requirement for increased computing capacity and efficiency in the post-Moore era, emerging computing architectures, such as in-memory computing and neuromorphic computing architectures based on memristors, have been extensively pursued and become an important candidate for new-generation non-von Neumann computers. We developed 40 nm reliable memristor technology on standard 12-inch process with high yield based on the materials and processes developed in the lab. This technology will serve as the key bedrock for the embedded memory, AI chips, neuromorphic systems and related industry. We further design and demonstrate highly efficient AI chips based on memristors using foundry-based memristor process, including a memristor based AI SoC incorporating RISC-V core. These chips demonstrate orders of magnitude higher energy efficiency than conventional CPU and GPU chips and hold great potential in reconfigurable AI applications. In particular, we extended the application of memristor CIM from pattern classification to ubiquitous optimization, where a memristor based universal Ising Machine is constructed, demonstrating great efficiecncy in solving combinatorial optimization problems.

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