Memrisys 2024

-Poster Session-

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Xiaoyuan Wang	Design of the tri-valued memristor and its application
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Yuan Fa	Volatile and Nonvolatile Resistive Switching in Wafer-Scale MoS2-based Memristors
Yujin Kim	Analysis of 3-Dimensional Gate-Injection Field Effect Transistor with VNAND Structure for Area-Efficient Neuromorphic Hardware

Analog weight update by tunable interfacial energy barrier by Li ion redistribution in Pt/p-$LiCoO_x$/p-NiO/Pt memristor for neuromorphic computing

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As the data-centric application, such as artificial intelligence, autonomous driving system and IoT, the demand for novel computing architecture increases due to the von Neumann bottleneck problems. From this point of view, neuromorphic computing is one of the promising new architectures. Neuromorphic computing emulates the human brain, which excels in complex tasks [1]. Unlike digital type computation in modern computer, neuromorphic computing employs analog synaptic weight for inference and learning process. To realize neuromorphic computing, artificial synapses which are essential elements for neuromorphic computing have been extensively investigated. For energy-efficient and high accuracy neuromorphic computing, a highly linear and symmetric weight update is important during potentiation and depression operation. Among the various candidates for artificial synaptic devices, two-terminal interface-type memristor is one of the promising devices due to its similar structure with biological neuron-synapse-neuron structure and precise and gradual resistance change in an analog manner [2]. In this study, Pt/p-$LiCoO_x$/p-NiO/Pt memristor is proposed as an artificial synapse for application to neuromorphic computing. This device employed p-type oxides and a high work function electrode (ex. Pt) to construct a low interfacial energy barrier to mitigate abrupt conductance change. In addition, fast and movable Li^+ ions were used to modulate the interface energy barrier between NiO and Pt bottom electrode. Using p-type oxides and fast movable Li^+ ions working as dopants, the device shows the highly linear and symmetric analog change in conductance at a low voltage with a high speed. Beside the linear and symmetric weight update, the memristor shows various synaptic behaviors such as dependence of weight update on the number of pulse application, paired pulse facilitation, and short-term and long-term plasticity. The conductance modulation is induced by the tunable interface energy barrier at NiO layer and Pt bottom electrode by redistribution of Li^+ ions within the NiO layer as well as supplied Li^+ ions from $LiCoO_x$ layer. These results demonstrate the potential application of Pt/$LiCoO_x$/NiO/Pt memristor to artificial synapses operated by voltage-driven Li^+ ion redistribution under the low energy barrier, realizing highly linear and symmetric weight update with a low voltage and high speed for energy-efficient neuromorphic computing systems.

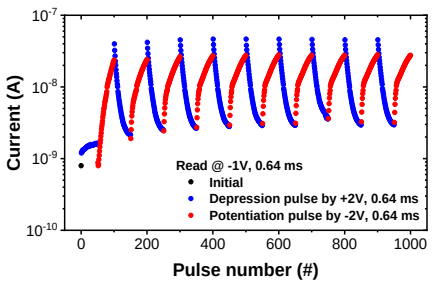

Figure 1. Weight update results of Pt/$LiCoO_x$/NiO/Pt memristor

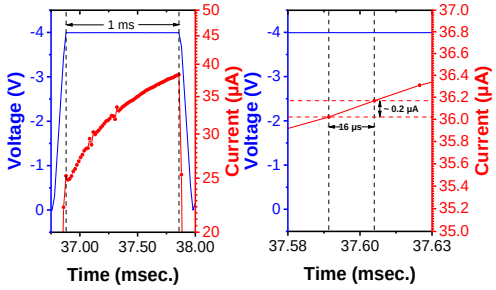

Figure 2. Operation speed; monitoring current change in real time during weight update

References

[1] J. Tang et al. *Adv. Mater.*, **31**, 1902761, 2019

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Heterogeneous Density-based Clustering with Dual-functional Memristive Array

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Recent data mining studies utilizing memristor-based crossbar arrays (CBAs) have employed various algorithms, including local hashing, data clustering, and dimensionality reduction. By leveraging the parallel vector-matrix multiplication (VMM) capabilities of CBAs, these systems operate more efficiently than traditional computing. However, previous studies faced limitations in fully implementing specific algorithms due to constrained device-level functionality. The data for these algorithms may have an analog or digital format, each requiring appropriate computing methods. This study proposes a new data clustering algorithm to overcome device- and algorithm-level limitations by fully utilizing the reconfigurable dual-mode (digital and analog) memristive CBA.

Conventional data clustering methods, such as k-means clustering and DBSCAN, inherently involve substantial computational overhead and struggle to effectively address local density variations within the data. To address this problem, this work introduces a new heterogeneous density-based clustering (HDC) algorithm to efficiently cluster datasets with varying densities using the parallel VMM operation of dual-functional CBAs. The processing method varies between analog and digital modes for data clustering on heterogeneous density datasets. In the analog mode, the Euclidean distance (ED) within the dataset is used to compute the local outlier factor (LOF) through analog domain VMM, enabling the detection of outliers. In contrast, the digital mode identifies clusters by evaluating connectivity between the detected outliers using digital domain VMM, thus considering local density in the clustering process. The proposed hardware-software co-developed algorithm feasibly clustered diverse synthetic datasets (~0.9 in adjusted rand index) that were impossible through conventional clustering algorithms. The protein structure was effectively confirmed using the single molecule localization microscopy (SMLM) dataset with various densities, demonstrating efficacy with real-world datasets. This study paves the way for efficient data clustering hardware in materials research, marking a significant advancement in the in-memory computing era.

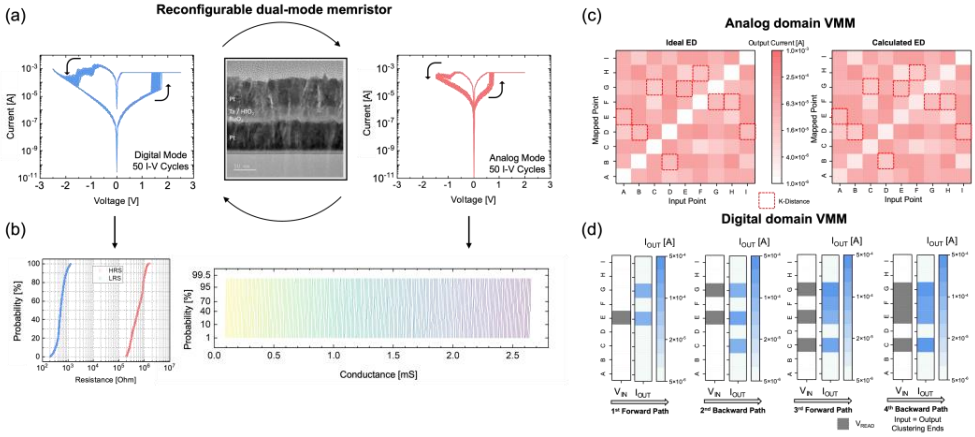

Figure 1. The dual-mode CBA characteristics and VMM operations. (a) Reconfigurable digital and analog mode characteristics. (b) State variation of digital mode and state tunability of analog mode. Implementation of (c) analog domain VMM for ED and LOF calculation and (d) digital domain VMM for locality-considered data clustering with proposed bidirectional propagation clustering method.

References

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Memimpedance-based Neural Adaptation Circuit with Hybrid CMOS/Volatile Memristor LIF Neuron

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Neural adaptation, allowing neurons to dynamically adjust their responses based on stimuli, significantly contributes to predictive coding, enhancing environmental selectivity, and maintaining neural systems at the edge of chaos [1], etc. The implementation of neural adaptation has aroused wide interest [2]; however, efficient implementation in hardware remains a challenge. In this paper, we propose a novel hardware implementation of neural adaptation based on hybrid CMOS/volatile memristor Leaky Integrate-and-Fire (LIF) Neuron Model, utilizing the observed memimpedance effect of memristors.

In Fig.1, we performed characterization for the memimpedance effect of our in-house fabricated HfOx-based memristors, using Keithley 4200A to realize specialized characterization pattern. The characterization flow includes two phases: 1. Applying multiple identical programming pulses to drive the memristor to different resistive state (RS). 2. Subsequently, applying a small AC signal of 0.5V, sweeping the frequency from 1kHz to 10MHz. RS is defined as the resistance under read pulses of 0.5V, preventing the device from switching. The cycle formed by the two phases is applied repeatedly, sweeping the voltage of the programming pulses in the first phase from 0.5V, 1V, 1.5V, ..., 6V, -0.5V, -1V, -1.5V, ..., -6V. The characterization results in Fig.1 are similar to the observation [3], where we can observe a clear positive correlation between RS and the capacitance in the memimpedance. In Fig. 2(a), the pulse source of the LIF neuron represents the input current received by the presynaptic membrane, while the Vout corresponds to the neuron spikes generated at the postsynaptic membrane. The current pulses integrated in the capacitor cause the Vout exceed the Vth of SnOx-based memristor, leading to the abruptly decrease in its RS and the Vout, forming a whole spike, as shown in Fig. 2(b). The spike is then propagating to the subsequent neuron. To realize neural adaptation, we replace the capacitor for integration in the LIF neuron with the HfOx-based memristor, to utilize the characterized memimpedance features for the integration with a time-varying integral coefficient (Capacitance). It allows the membrane Vth gradually to increase, leading to a progressively shorter output spikes until saturation. In Fig. 3, the simulation results in Cadence that is resemble to the biology neural adaptation [1] indicates the firing intensity descend with prolonged and repetitive stimuli.

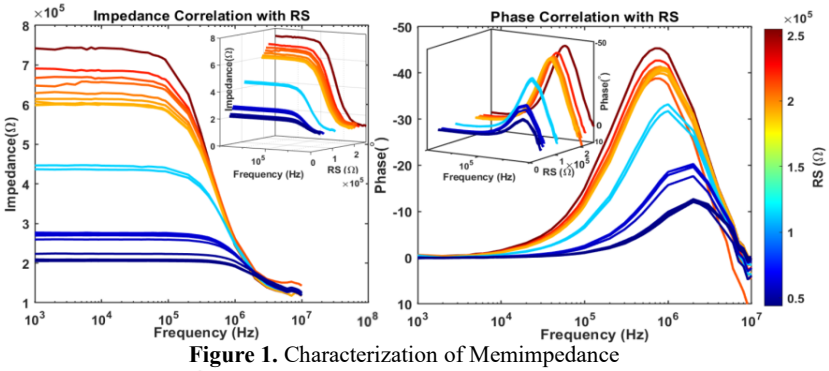

Figure 1. Characterization of Memimpedance

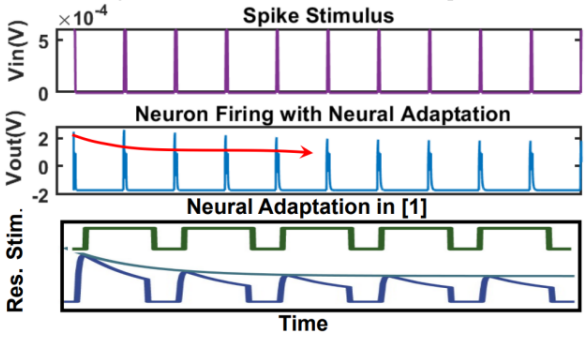

Figure 3. Simulation Results of Neural Adaptation

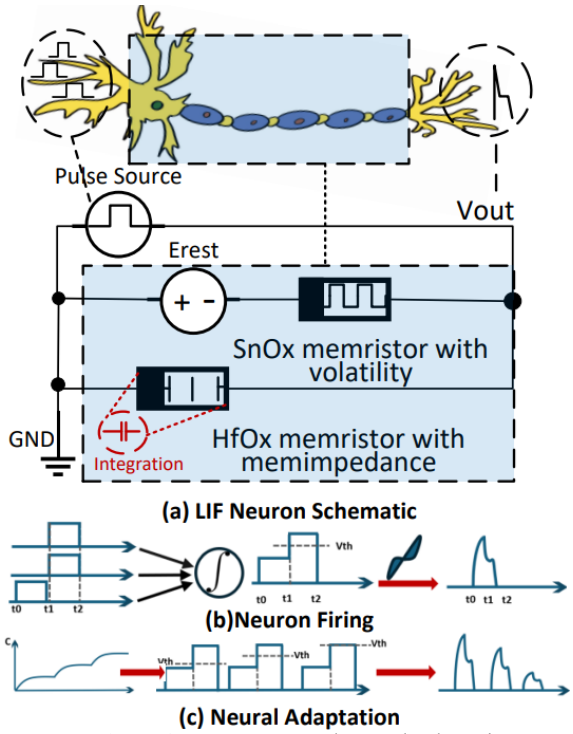

Figure 2. LIF Neuron and Neural Adaptation

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[2] Ganguly, C. et al., *Commun. Eng.*, 3(1), 22, 2024.
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Reservoir computing using graphene-based solid state electric double layer transistors

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Recently, the rapid development of AI technology has confronted serious problems such as increasing computational costs and increasing power consumption. Physical reservoir computing (PRC) is a form of physical implementation of machine learning that is suitable for efficiently processing time series data and has the possibility to resolve the problems. It utilizes nonlinear dynamics of physical phenomena in materials or devices for information processing. In this context, PRC has been studied using various physical phenomena such as optical response and magnetic spin. Previously, our team developed ion-gating reservoirs (IGRs) using solid-state ionic materials, such as electric double layer (EDL) and redox-based transistors.[1-5] In this study, we tackled improving the PRC performance of EDL transistor-based IGRs by focusing on the channel material.

We used a monolayer graphene deposited by chemical vapor depositions as the channel semiconductor with Au/Cr source and drain electrodes. Then, an electric double layer transistor (EDLT) was fabricated by depositing a Li^+ -conducting amorphous solid electrolyte (Li-Nb-O) and a gate electrode ($LiCoO_2$) by pulsed laser deposition, as shown in Fig.1. Applying various V_G to the gate electrode causes Li^+ transport inside the electrolyte. The formation of EDL at the graphene channel/electrolyte interface changes the electron carrier density in graphene, and the I_D through the channel can thus be controlled. We evaluated the electrical characteristics of this transistor and its performance as a PRC device through a benchmark task.

The I_D-V_G characteristic measured by sweeping the V_G from -1.5 V to +1.5 V is shown in Fig. 1. When a negative V_G is increased (e.g., V_G < -0.2 V), Li^+ moves toward the gate electrode, and holes are injected into the channel surface, forming an EDL (p-type conduction) and vice versa. The performance of this EDLT was evaluated by the 2nd-order nonlinear autoregressive moving average (NARMA2) task, which is a time-series data prediction task requiring nonlinearity and short-term memory and is thus widely used as a typical benchmark task of PRC. The performance is evaluated by the value of the normalized mean square error (NMSE) with the nonlinear transform output (predicted waveform) of the PRC and the target (i.e., a low NMSE means high performance). The predicted waveform by the EDLT reproduced the characteristics of the target waveform well (Fig.2), indicating that it predicted the time-series data with high accuracy. The NMSE (the test phase) was 0.015, which was notably lowered by 40% compared to the high-performance diamond-EDLT (NMSE: 0.020 in the test phase) [1] The high performance is attributed to the unique I_D-V_G and transient characteristic of the ambipolar EDLT. This work was supported by JST PRESTO (grant number, JPMJPR23H4).

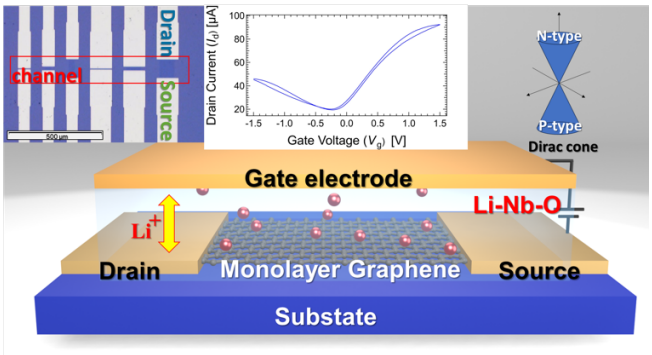

Figure 1. Schematic image of an EDLT and the I_D-V_G

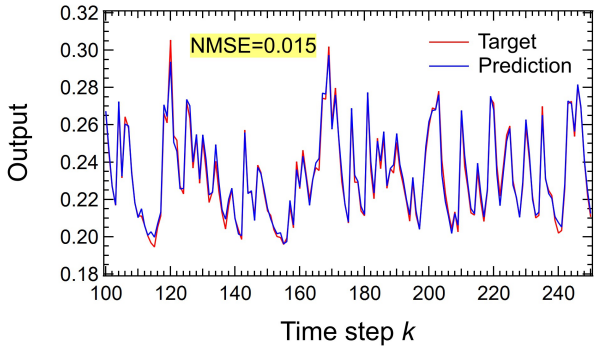

Figure 2. Target and prediction waveforms of the NARMA2 task

References

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Neuromorphic Computing based on Two-terminal Au nanoparticle Floating-gate Memristor

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The majority of computers have been built based on the von Neumann architecture because it has powerful advantages. However, with the advent of the big data era, von Neumann bottleneck occurs due to the limitations of the physical structure. Neuromorphic computing, which mimics human brain function by creating a circuit that mimics the shape of neurons, is one of the ways to solve the above problem.

In this study, we demonstrated Neurosynaptic array based on two-terminal au nanoparticle floating-gate Memristor (AuNp-FGM). By forming au nanoparticles between tunneling oxide and floating gate, the device can operate lower than ±3V region. Using the change of the fermi level (E_f) of graphene, AuNp-FGM exhibits memory characteristics. The device exhibits high on/off ratio over than 107, retention longer than 9 hours, and robust endurance more than 80,000 times. Also, AuNp-FGM shows low cycle to cycle variability of C_v = 3.6% (n=90, $C_v = \sigma/\mu$, σ = standard deviation, μ = mean value). Furthermore, AuNp-FGM shows almost linear update characteristics, for 100 level potentiation (+4V, 0.4s), nonlinearity factor ranged from 0.1 to 0.6. For 100 level depression (-3V, 0.2s), it ranged from 2.3 to 4.6 (n = 15), indicating excellent applicability for neuromorphic computing. A similar trend was also observed even when the number of input pulses was changed (50, 100, 200, 300, 400 inputs)

Based on AuNp-FGM, we fabricated a neurosynaptic array, consisting of 18 neurons and 288 synapses. Four types of data (‘A’, ‘B’, ‘Y’, ‘Z’) were used in 90 times learning simulation, 2 neurons and 32 synapses were used to learn one alphabet. The training results were confirmed by measuring the output current of the neurons which is connected to the trained synapses, we were able to successfully trained each alphabet on the neurosynaptic array.

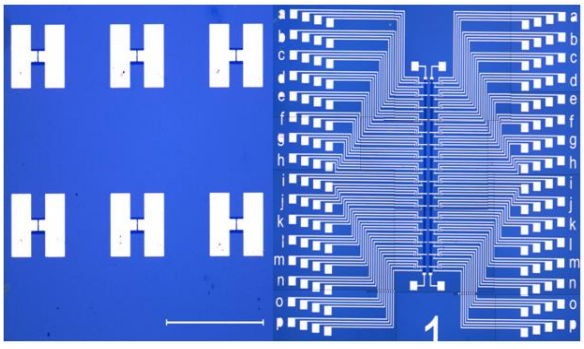

Figure 1. OM image of AuNp-FGM (left, scale bar = 1mm), OM image of Neurosynaptic array (right)

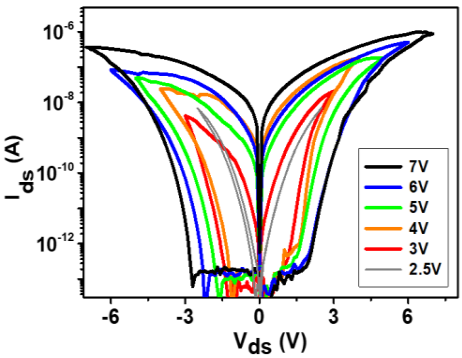

Figure 2. I_{ds}-V_{ds} characteristic of AuNp-FGM

References

[1] Vu, Q., *et al.*, *Nat. Commun.* **7**, 12725 (2016).
[2] Q. A. Vu, et al., *Adv. Mater.* 2017, 29, 1703363.
[3] Won, U.Y., *Nat. Commun.* **14**, 3070 (2023).

Artificial retina technology plays a crucial role in the field of artificial intelligence, particularly in the domains of fast static target recognition and trajectory detection. However, the current challenge lies in the absence of highly sensitive, reconfigurable, and large-scale integrated retinal devices, hindering the development of fully functional artificial retinal hardware. In this study, we introduce a groundbreaking monolithically integrated 409600 pixel perovskite optoelectronic sensor array. By utilizing indium gallium zinc oxide thin film transistors and perovskite photodetectors to mimic the anatomical structure of the biological retina, we have achieved a 1T-1PD pixel with broadband and reconfigurable characteristics. Notably, this structure demonstrates rapid photoelectric response capabilities under reverse-biased conditions for sensitive photoelectric detection tasks, while exhibiting continuous photoconductivity effects in forward-biased mode for trajectory tracking detection tasks.

Silicon/Graphene Optical Sensors and Neuromorphic system for Visual Cell Emulation

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In the field of solar energy, next-generation Schottky solar cells incorporating graphene, a two-dimensional material, are gaining significant attention due to their high efficiency and open-circuit voltage (VOC) [1]. The unique ability of graphene-based solar cell devices to convert light into electrical energy positions them as ideal candidates for replicating the functionality of human visual cells [2].

This study investigates the creation of a biomimetic device that emulates the complex processes of the human retina, including the formation of visual information, its conversion into electrical signals by photoreceptors, and the subsequent transmission of these signals to the brain via the optic nerve. The device aims to simulate the visual cortex's role in object recognition. By integrating a comparator, we achieve a hardware component of the vision neural network, where the modulation of spike numbers in response to varying light intensities mimics the human perception adjustment (Figure 1).

The simulation of the visual cortex's function was conducted using Conventional Neural Network (CNN) modeling in MATLAB. The simulations employed the MNIST dataset (pixel size: 28x28) to compare the performance of existing analog and digital signals, achieving a peak accuracy of approximately 75% after thirteen iterations (Figure 2).

This study demonstrates the feasibility of a neuromorphic integrated visual system that closely mimics the human visual system. Building upon this foundation, future research will focus on developing an advanced visual system that operates similarly to the human brain by connecting our own floating gate memristor to the visual sensor described in this study [3]. The spike information generated by the visual sensor will be transmitted to the memristor, following the principles of spike-timing-dependent plasticity (STDP), instead of using a comparator. Memristors have the capability to learn and store transmitted information, functioning akin to real neurons through the leaky integrate-and-fire (LIF) mechanism.

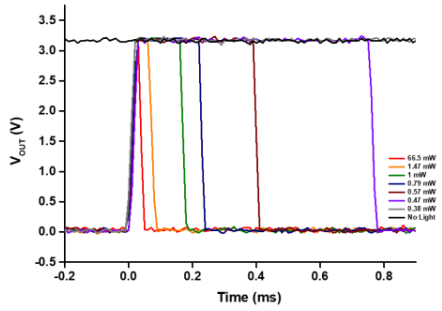

Figure 1. Output spikes according to the laser intensity

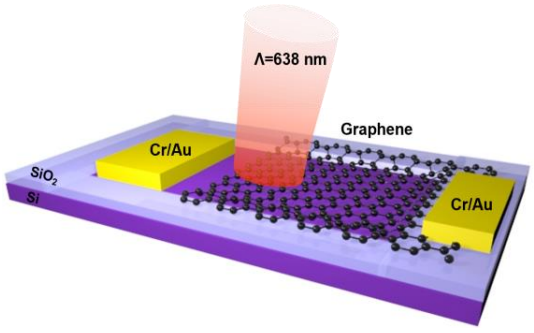

Figure 2. Schematic image of Silicon/Graphene Optical Sensor

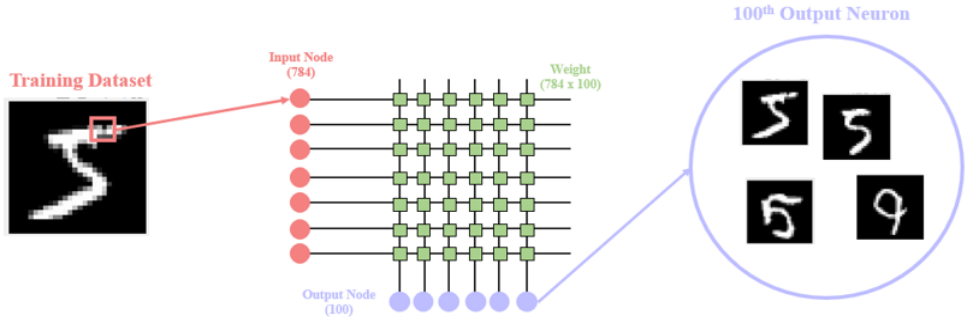

Figure 3. Schematic image of SNN system using the 28*28 MNIST dataset

References

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Physical Reservoir Computing with Percolating Networks of Nanoparticles

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The network of neurons and synapses that comprises the biological brain enables natural information processing with remarkable efficiency [1]. Percolating Networks of Nanoparticles (PNNs) consisting of metallic nanoparticles (Figure 1) are complex self-assembled nanoscale systems that possess many brain-like attributes and are therefore appealing for neuromorphic computation [2].
Additionally, PNNs are fabricated with straightforward cost-effective processes and have remarkable longevity [3].

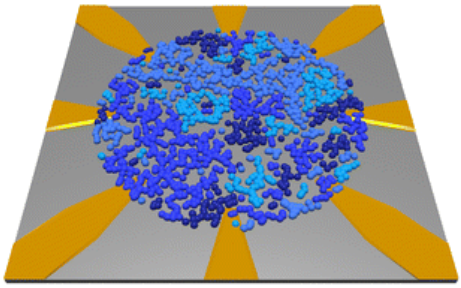

Figure 1. Schematic of a Percolating Network of Nanoparticles (PNN) with multiple gold electrodes. The different particle colours represent individual groups of well-connected particles separated by memristive tunnel gaps.

Previously we have shown via simulations that PNNs, constructed from networks of memristive tunnel-gaps and acting as reservoirs within a reservoir computing (RC) framework, can successfully perform computational tasks such as NARMA, Memory Capacity, Non-linear Transformation, and Waveform Discrimination [4]. Here, we demonstrate experimentally that our PNNs solve the more practically relevant task of spoken digit recognition. After suitable pre-processing steps, our PNN transforms signals to a higher dimensional space, allowing prediction of the spoken digit. We achieve a high classification accuracy on the TI-46 dataset [5], comparable with the best performance achieved with other physical RC systems. We further show that our system achieves state-of-the-art accuracy on the larger and more challenging Free Spoken Digit Dataset (Figure 2).

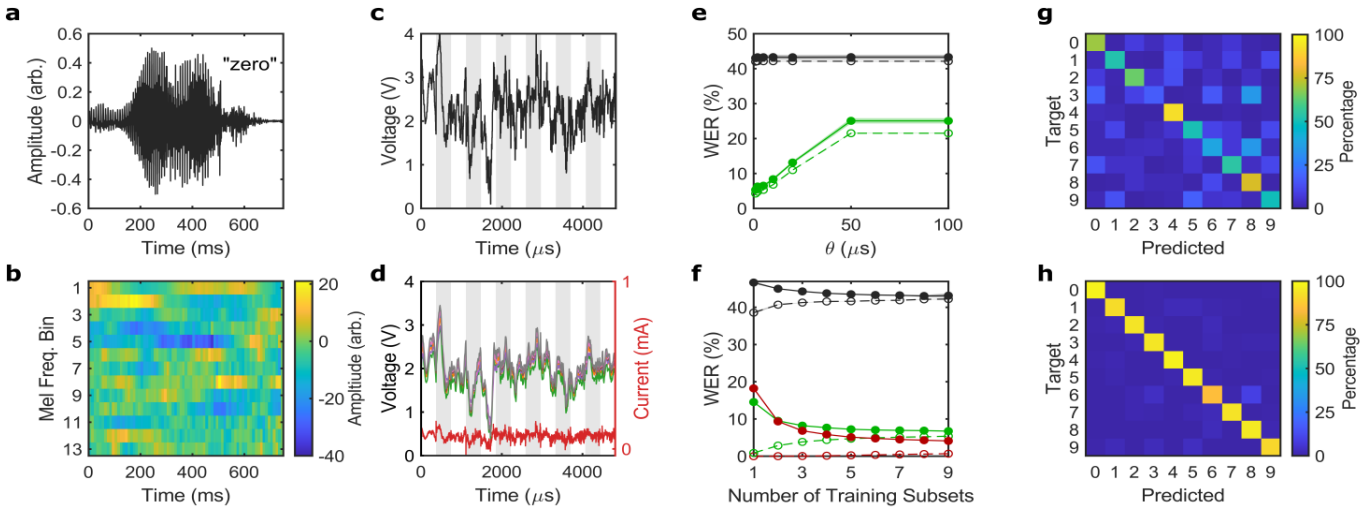

Figure 2. Spoken Digit Recognition. (a-c) Preparation of the spoken digits to an appropriate signal for our PNN. (d) The transformed signal measured from the PNN. (e-h) Final classification accuracy of the spoken digits.

References

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Cluster type selector-less 1R memristor array for spiking neural network

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A memristor holds great potential as a next-generation device, but device-level performance improvements and large-scale array implementation are necessary for various emerging applications. The switching characteristics and performance of memristors are predominantly determined by mobile species or redox reactions and the consequent formation of conductive paths. However, controlling the redox reaction is challenging, making it difficult to manage the precise growth and rupture of the conductive path, significantly degrading the switching characteristics. Furthermore, the well-known conventional ion-based switching behavior does not have inherent non-linearity due to the formation of continuous conductive filaments, so further development of an external selection device and verification of its compatibility are required, which makes the practical application of memristor arrays difficult.

Therefore, in this study, we propose a nanorod-based memristor, Pt/SiO_2 nanorods/Ru, to enhance switching characteristics by controlling the ion dynamics, such as activation energy, mobility, and redox reaction. By introducing a nanorod structure, the dominant movement towards the surface with relatively lower activation energy for diffusion leads to increased mobility, and the concentration of electric fields due to structural characteristics promotes redox reactions. This approach leads to efficient ionization and increased ion mobility, resulting in electroforming-free operation, low power consumption, and high uniformity. Additionally, the ion supply can be precisely controlled, enabling high linearity in conductance modulation and forming the different types of conductive paths from the conventional filamentary memristor, leading to inherent non-linearity in the On-state. These memristors were successfully integrated into a 16 x 16 selector-less crossbar array, demonstrating high uniformity and an 80% MNIST recognition accuracy when simulated using a Spiking Neural Network (SNN), underscoring their potential for efficient neuromorphic computing and AI applications.

Energy efficient, high performance resistive memory device with Ag/VO_x/Pt structure by facilitated Ag filament formation

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Nowadays, conventional von Neumann computing systems face significant bottlenecks in processing speed due to data assessment between processor and storage for data-intensive applications. The data movement including the transfer from off-chip to on-chip incurs substantial costs in terms of bandwidth, energy, and latency—far more than computation itself. Furthermore, energy consumption is a major constraint in the conventional computing systems. These issues are especially pronounced in today's data-intensive servers and mobile systems. In addition, conventional memory device technology is facing numerous challenges in technology node scaling, reliability, energy efficiency, and performance enhancement. Thus, breakthroughs in memory devices for new computing systems are highly required. In these circumstances, emerging non-volatile memories (NVMs) such as resistive random-access memory (RRAM) are gaining attention for their potential as computing elements in processing-in-memory (PIM) systems, due to their potential simple structure and high performance. To achieve high performance and reliability in RRAM devices, it is crucial to explore suitable switching oxide materials and structural modulations.

Among various oxides for RRAM, vanadium oxide (VO_x) exhibits proper properties as resistive switching element such as high metal cation diffusivity such as Li^+, Zn^{2+}, Na^+, K^+ ions. As well as it enables to serve as a great cathode material in both crystalline and amorphous phase for the lithium-ion batteries (LIBs) or aqueous zinc-ion batteries (aqZIBs) [1–5], it can make vanadium oxide promising electrolyte for metal filament-type RRAM operating through the formation and dissolution of conductive filaments consisting of metal atoms within a solid electrolyte.

In this study, the resistive switching properties of Ag/VO_x/Pt structured device is investigated for the application to high performance computing systems. DC voltage sweep measurements reveals average V_{SET} and V_{RESET} values of +0.23 V and −0.07 V respectively, with a low I_{RESET} of less than 1 mA, along with forming-free characteristic. The switching speed is less than 100 ns in pulse measurements. Furthermore, the device exhibits narrow cell-to-cell (C–C) and device-to-device (D–D) distributions. Almost complete retention for more than 12 hours at room temperature is achieved. These features—forming-free, low operation voltage, fast operation speed, uniform cyclability, and long memory retention—can take advantages when this device is implemented as processing elements in PIM architecture. In addition to enhanced electrical properties, a noticeable two-step resistance change is observed at SET pulse operation. Upon the application of SET pulse, the resistance partially decreases to middle resistance state (i.e., transient resistance state). After several hundred nanoseconds, it further decreases to reach the low resistance state once the filament formation is complete. The two-step resistance change in a staircase-like form is interpreted to be associated with the clustering of Ag atoms within VO_x layer followed by Ag filament formation. The facilitated formation and rupture of Ag filament within an oxygen-deficient VO_x layer eliminates the need for a forming step. Moreover, the amorphous structure of VO_x layer, abundant with oxygen vacancies, significantly enhances Ag^+ ion migration, thereby facilitating filament formation and stabilizing uniformity. These results highlight the potential of Ag/VO_x/Pt device as non-volatile computing elements which is suitable for PIM applications.

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Stochastic Ion-motion Mediated Volatile Threshold Switching Memristor Enables Probabilistic Computing

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Recently, quantum annealing (QA) machine has been utilized to solve combinatorial optimization problems (COPs), which typically exhibits exponential time complexity, within a reasonable scale of execution time. Despite the dramatic improvement in problem-solving capability offered by QA, extremely low temperatures for operation, leading to high power consumption and operational difficulties are pointed out as critical disadvantages. To breakthrough aforementioned drawbacks, probabilistic computing has been proposed as an attractive approach to solving COPs by mimicking QA at room-temperature using the probabilistic output of electronic devices. For its implementation, it is essential to develop devices that are inherently stochastic and capable of generating outputs at high speed with a probability proportional to the input bias. Additionally, constructing the simplest unit component, known as a probabilistic bit (p-bit), which includes the device and refines its output, is necessary. However, reported implementations of probabilistic computing with p-bit so far involve devices with complex structure and additional component such as transistor, or demonstrate simulations based on the characteristics of a single p-bit.

Meanwhile, we note that ion-motion mediated memristors with volatile threshold switching (TS) characteristics demonstrate significant cycle-to-cycle (C2C) variation under the applied arbitrary pulse train. Moreover, the device's turn-on probability increases proportional to the pulse amplitude. This behavior occurs because an increase in electrical bias accelerates ion-motion, causing the conductive path inside the device to grow without precise confinement of formation spot. Therefore, this bias-dependent controllable probability and stochastic property make TS devices one of the most promising candidates for a p-bit.

In this study, we fabricated a vertical Metal-Insulator-Metal (MIM) structure TS device using Pt/Ag/SiO_2/Ag/Pt. The device exhibits a low threshold voltage ($\approx \pm 0.2$ V) with C2C variation, an ultra-low OFF state current (< 10 pA), and a high ON/OFF ratio (> 10^7). Furthermore, by adopting a nanorods-based (NRs) switching layer, we achieved remarkable switching speed improvement, which contributes to a higher bit generation rate for the TS-based p-bit. Additionally, it was confirmed that the generated probabilistic output depends on the amplitude of the input pulse, successfully forming a sigmoid fitting curve, a representative characteristic for application in probabilistic computing. It is believed that the NRs-TS device and the accompanying p-bit shown in this work are suitable for low-power and high-speed probabilistic computing applications.

Size-Dependent Study on Nanosized VO_2 Phase Change Memory Devices.

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Volatile Mott memristors are key components of neuromorphic circuits alongside conventional non-volatile resistive switches. While the latter essentially plays the role of artificial synapses in neural network applications, the former act as artificial neurons implementing several neural spiking patterns [1]. In addition, Mott memristors are well applied to oscillating neural networks, where information processing occurs in the dynamic domain, and the computation is encoded by the phase of the oscillators, all these applications require fast operation. In our study, we fabricated devices with varying ultrasmall (≈ 20-100 nm) spacing between the contacting electrodes. The asymmetric, V-shaped electrode arrangement focuses the switching region into a well-defined spot [2], enabling us to analyze the device operation as a function of the device size. By applying time-resolved measurements, we also revealed the switching dynamics. switching dynamics. The simplified spatial structure of the active volume also facilitates the device modeling. From this inspiration, a two-dimensional resistor network model was employed to simulate the size-dependent and dynamic behavior of our nanosized VO_2 memory devices.

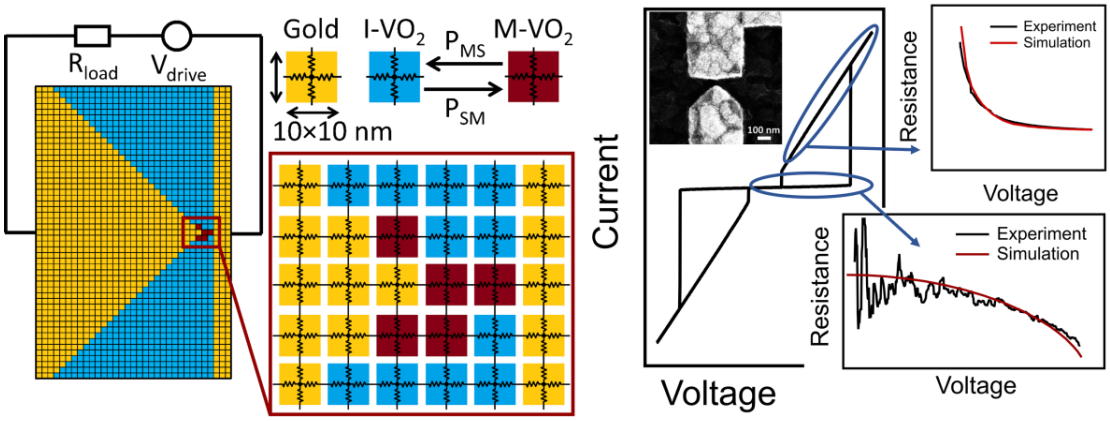

Figure 1. Left panel: Schematic of our two-dimensional resistor network model using realistic electrode geometry. The active region is modeled as an array of cells, each of which can be either insulating (I-VO2, blue) or metallic (M-VO2, red) state. The phase transition is considered a thermally activated process, with transition probabilities of the cells (P_{IM} (T) and P_{MI} (T)) depending on the temperature. **Right panel:** Switching I(V) trace of the nanogap device. The two inset panels show the measured (black curves) and simulated (red curves) R(V) characteristics of high resistance OFF state (bottom panel) and low resistance ON state (top panel).

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Improved Stateful Logic Designs based on Memristive 1T-1R Arrays

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Memristive Devices have recently gained attraction for the implementation of Computing-in-Memory (CIM) and especially their potential in stateful logic concepts such as Memristor-Aided Logic (MAGIC). Originally proposed for passive crossbar structures, modern concepts integrate these operations by combining memristive elements together with traditional CMOS transistors, which improves the reliability regarding sneak path currents. However, as stateful memristive concepts rely on the conditional switching of a memristive device, they are prone to variability, which arises from the inherent memristive switching mechanism and its stochasticity. Additionally, the high amount of operation parameters, namely pulse voltages/duration, initial resistances states, logic inputs and the switching polarity, further increase the complexity of the operation.

To address these challenges, we introduce a robust framework to evaluate the switching-dependent error rates of stateful memristive logic concepts focusing on active 1T-1R structures [1]. Based on the framework results, we identify critical operations parameters and, for the first time to our knowledge, we demonstrated the successful execution of MAGIC operations in hafnium-based integrated 1T-1R devices. By adjusting the operation voltages, we achieved experimental operation success rates up to 100% [2].

Based on the observations of stateful logic in simulation and measurement, we propose two novel extensions for improving the original stateful MAGIC concept: 1) the combination of stateful and non-stateful logic elements for concatenated Boolean operations. Specifically in active 1T-1R structures, the transistor gate voltage can be exploited as second, volatile, input to tune the 1T-1R series resistance. This approach extends the number of logic inputs from 2 (stateful MAGIC) to 4 (combined stateful/non-stateful) per operation which significantly reduces the required number of cycles. 2) a 1T-1R Three-Memristor Stateful Logic approach, which extends the executable primitive logic functions with only a minimum of additional circuitry.

Inputs	**SR** *VSet* 1.0 V *Vgate* 1.5 V	**SR** *VSet* 1.2 V *Vgate* 1.5 V	**SR** *VSet* 1.0 V *Vgate* 1.7 V
00	**0**	**0**	**0**
01	**38**	**41**	**100**
10	**55**	**27**	**99**
11	**94**	**88**	**100**

Table 1. Experimental voltage-dependent 1T-1R MAGIC success rates (SR)

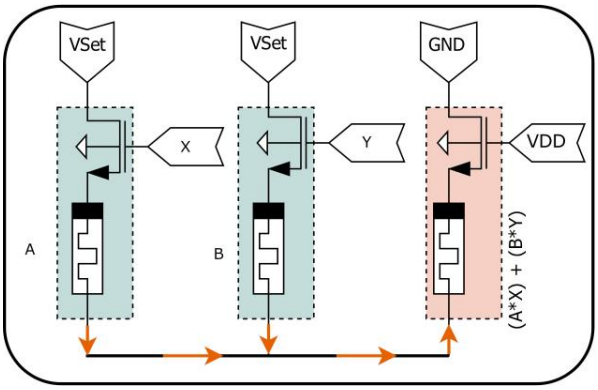

Figure 1. Circuit Diagram for combined stateful (A,B) and non-stateful (X,Y) logic inputs as MAGIC extension

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Computational performance of Magnonic Reservoir Computing with Increased Number of Detectors

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Reservoir computing addresses concerns over power consumption and computational costs in machine learning. It enables fast learning with low power consumption and computational costs. By using a device with nonlinearity, short-term memory, and high dimensionality, physical implementation is possible. In particular, it was theoretically predicted and experimentally verified that spin wave interference can perform highly efficient reservoir computing, demonstrating improved performance with up to two spin wave detectors.[1,2,3] Furthermore, while simulations have shown that increasing dimensionality through two or more multiple detections can improve computational performance,[4] the effects of using more than two detectors on the computational performance through high dimensionality enhancement remain unclear. In the study, we evaluated the computational performance experimentally by increasing the number of detectors to six and utilizing nonlinear interference effects.

We used a magnonic device with $Y_3F_5O_{12}$ single crystal, as shown in Fig. (a), to perform one of the most important prediction benchmark tasks from the Nonlinear Autoregressive Moving Average (NARMA) model. In this study, we increased the number of detectors to six to improve computational performance through a significant increase in the number of detections and experimental nonlinear interference effects. We evaluated the prediction error of NARMA10, which requires short-term memory up to 10 steps with the external applied magnetic field and input pulse interval as measurement conditions. First, to determine the two terminals used for input, we selected the two terminals from the six terminals indicated in Fig. (a) and conducted a total of 15 measurements. The detection terminals used were terminals A and B, as indicated in Fig. (a). As shown in Fig. (b), When terminals 3 and 5 were used as input terminals, the comparison between the target waveform and the output waveform during testing under the conditions of a magnetic field of 178 mT and a pulse interval of 25 ns shows a good match, at that time, the error was 0.155 during the testing phase. When the number of detections was virtually increased to four, as shown in Fig. (c), the computational performance changed with respect to the magnetic field and pulse interval, resulting in an improvement in the best score under the same conditions as with two detections. This work was partially supported by the Innovative Science and Technology Initiative for Security Grant Number JPJ004596, ATLA, Japan, and JST PRESTO (JPMJPR23H4).

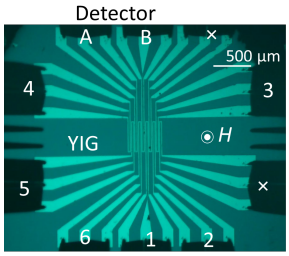

Fig. (a) The optical microscope photograph of the device.

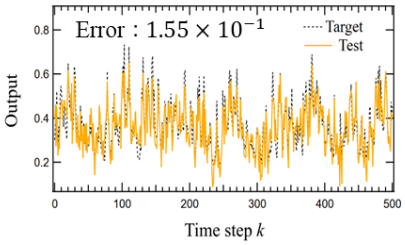

Fig. (b) Comparisons of target and output waveform at testing phases.

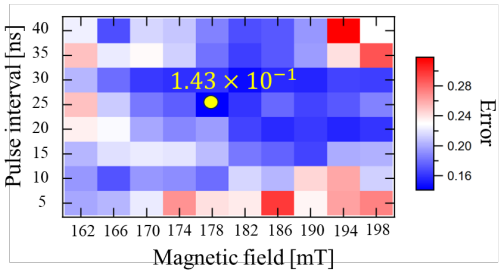

Fig. (c) Prediction error variation under various measurement conditions. (using four virtual detections)

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Circuit emulating neuronal response based on Ga_2O_3 photomemristors

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Gallium oxide-based memristors were introduced as component of a circuit emulating a neuronal membrane to investigate its nonlinear operation and sensitivity to electromagnetic radiation in the visible spectral region. While the former characteristics is employed on digital memory and logical circuit development, the latter has attracted interest for biological and neuromorphic system applications. Gallium oxide (Ga_2O_3), which has five main crystalline phases, is a transparent semiconductor material with band gap around 4.5 - 4.9 eV. It has been observed that substrate temperature plays an important role during the deposition process of thin films, such as crystal phase selectivity and optoelectronic properties [1]. In this work, testing devices were produced from films deposited, by IBAD (Ion Beam Assisted Deposition) on p-type Silicon substrates, at room temperature and ~400 °C. Aluminum contacts were evaporated over the thin film surface and on the substrate back surface. Films deposited at lower temperatures predominantly have β-phase, while those deposited at higher temperatures have dominant ε-phase, as verified by X-ray diffraction. The memristors were characterized by voltage-current analysis. The current-voltage measurement of isolated device provided key information for understanding the memristor operation, revealing its unipolar characteristic and responsiveness to light (Figure 1). Therefore, the tested devices are, in fact, photomemristors. In the neuromorphic circuit measurement, the aim is to use the circuit that emulates a neuronal membrane and study the memristors behavior. It was proved to be an excellent tool for observe action potentials. There are prospects for applications that mimic human vision. In a biological system, information in the brain is transmitted through electrical and chemical impulses, generating an action potential. In this experiment, as depicted in Figure 2, a PWM (Pulse Width Modulation) signal is responsible for emulating the behavior of the action potential. However, as observed in the curves, memristor under illumination with LEDs of different wavelengths induces modifications in the signal. The measurement was conducted on an equivalent resistance to serve as a reference for comparison.

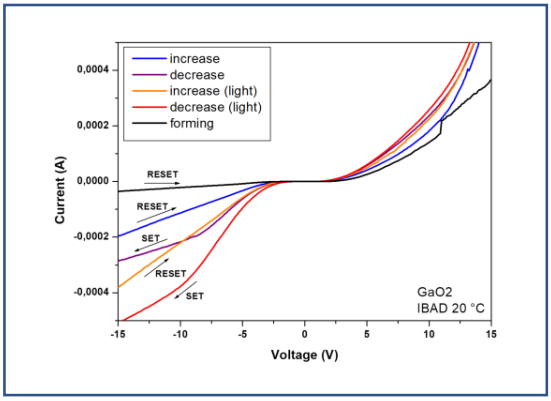

Figure 1. Hysteresis shift influenced by the incidence of light

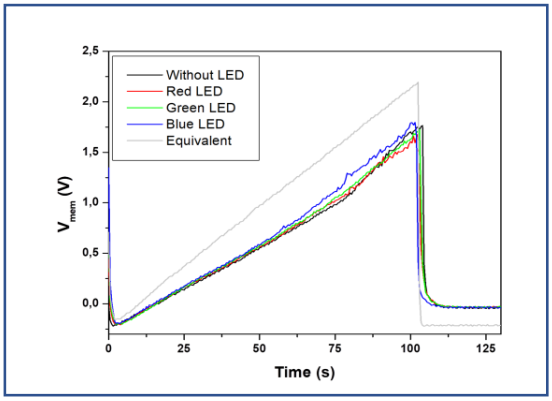

Figure 2. Action potential emulation with different illumination conditions

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Self-rectifying Two-terminal Vertical Floating Memristor

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High-performance artificial synaptic devices are essential for developing energy-efficient neuromorphic computing systems. Consequently, various types of memristive devices are being studied. Among these devices, RAM has a vertical two-terminal structure with two electrodes, which allows for a high memory integration[1],[2]. In contrast, floating gate memristors have only been researched in a horizontal two-terminal[3] or three-terminal structure[4],[5], which leads to low memory integration. To overcome this issue, we propose a two-terminal vertical tunneling random-access memory (VTRAM). VTRAM has a vertical structure of ZnO/Au/Al_2O_3/Pt/Al_2O_3/Au, where ZnO, Al_2O_3 and Pt serves as the channel, insulator, and floating gate respectively. VTRAM exhibits both self-rectifying and non-volatile memory effects simultaneously. This self-rectifying effect can suppress sneak currents when crossbar array is fabricated, reducing the need for additional selectors and increasing integration density. Our VTRAM shows rectification ratio of 10^5 for the self-rectifying behavior and on/off ratio of 10^7 for the memory behavior. Furthermore, VTRAM has long retention time over 10,000 s and stable switching cycle of 10,000 times.

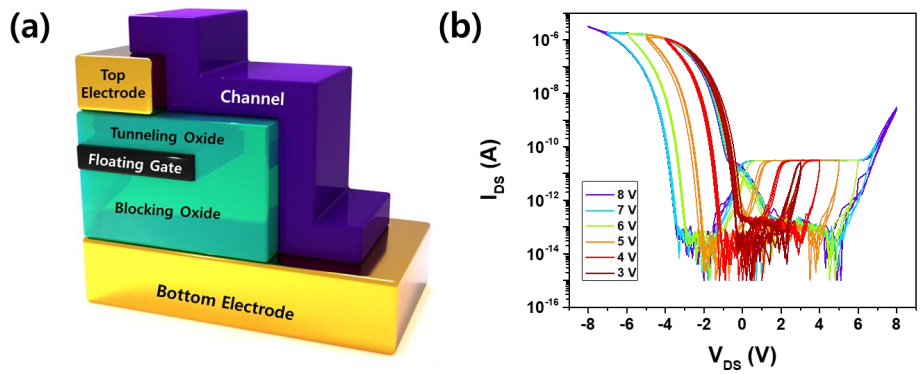

Figure 1. (a) Structure of VTRAM (b) I-V curve of VTRAM measured by varying the voltage sweep ranges from 3 to 8 V

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Reconfigurable Non-volatile Floating Gate Memory based on van der Waals Heterostructure for Multi-functional Devices

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Bio-inspired computing, which mimics the functionality of biological neural networks, offers a promising solution to the von Neumann bottleneck.[1,2] This bottleneck arises from the necessity of transferring data between memory and processing units, leading to redundant information processing and increased power consumption.[3] Floating-gate memory devices based on two-dimensional materials exhibit long-term synaptic plasticity with both electrical and optical stimuli.[4-6] However, they face challenges in achieving reconfigurability for multifunctional applications. In this study, we introduce a reconfigurable non-volatile floating gate memory based on a graphene floating-gate, h-BN insulating layer, and tungsten diselenide semiconductor (Gr/h-BN/WSe_2) heterostructure. By modulating the asymmetric source and drain contacts, we achieve both n-type and p-type non-volatile memory behaviors (Figure 1). The coupling of electrical and optical stimuli in the synapse enables hetero-synaptic plasticity, with relaxation timescales tunable via light intensity or control-gate voltage. This novel structure of asymmetric floating gate memory devices holds significant potential for integration into sensor-memory and computing applications, paving the way for advancements in modern electronics.

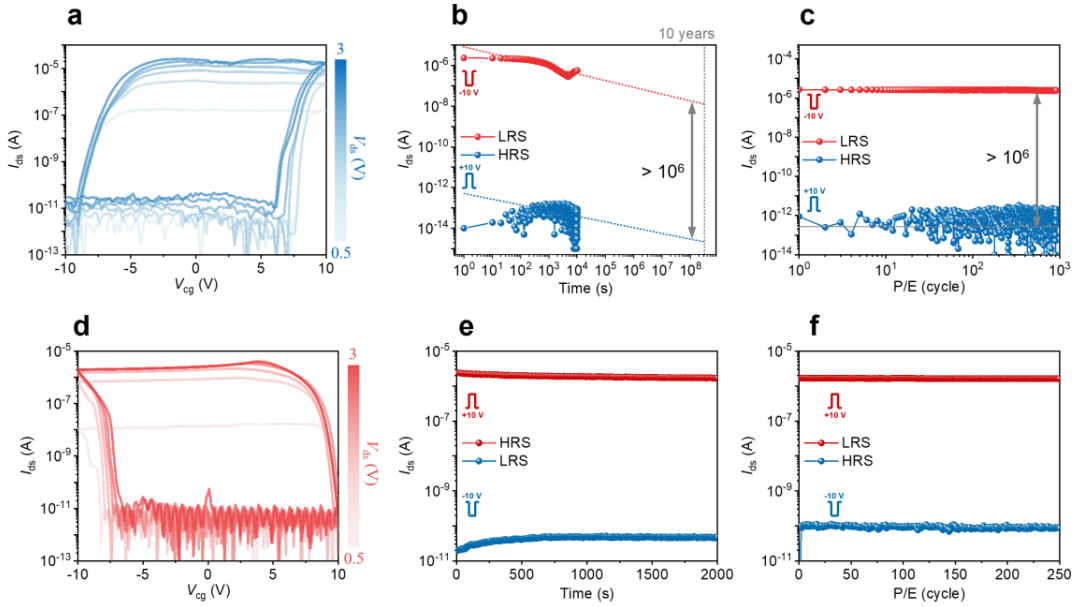

Figure 1. Reconfigurable floating gate memory based on Gr/h-BN/WSe_2 heterostructure. (a-c) Transfer characteristics showing the n-type memory window, retention, and endurance of the n-type floating gate memory, respectively. (d-f) Transfer characteristics showing the p-type memory window, retention, and endurance of the p-type floating gate memory.

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Development and Resistive Switching Properties of Amorphous GaO_x Four-Terminal Crossbar Memristor

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Background: An amorphous GaO_x (a-GaO_x) memristor is promising in terms of exhibiting non-filamentary type resistive switching properties as well as the feasibility of high-temperature operation.[1] Recently, we have been developing four-terminal planar memristor devices using a-GaO_x to mimic higher-order synaptic (or hetero-synaptic) characteristics that are difficult to obtain with conventional two-terminal devices.[2] However, the planar devices are limited to achieve high-density integration. In this study, we report the fabrication and characterization of prototypic four-terminal crossbar memristor devices using a-GaO_x. The present device provides a fundamental unit of integrated four-terminal crossbar array memristor architectures.

Experimental Method: Four-terminal crossbar memristor was fabricated on SiO_2/Si substrates (Fig. 1(a)). We used electron beam lithography and lift-off processes to pattern each layer of the device. The Pt/Ti layer for the bottom electrode (T3) and Pt for the gate electrodes (T2, T4) were deposited using electron beam evaporation. The memristive a-GaO_x layers (M1, M2) and the ITO layer for the top electrode (T1) were deposited using a pulsed laser deposition under a low-pressure argon (2.0 Pa) and oxygen (3.5 Pa) atmosphere, respectively. Plan-view scanning electron microscopy (SEM) and cross-sectional transmission electron microscopy (TEM) images of the crosspoint in our fabricated four-terminal device are shown in Figs. 1(b) and 1(c), respectively.

Experimental Results: Figure 2 (a) shows the voltage application protocol for measuring resistive change characteristics. Write voltages $V_{2,4}$ were simultaneously applied to T2 and T4 for 5 s while T1 and T3 were grounded. Then $G_{1\text{-}3}$, the conductance value between T1 and T3, was measured by applying a read voltage V_1 of 1 V to T1 for 50 ms while T3 was grounded. This cycle was repeated by changing $V_{2,4}$ in the range between the minimum voltage value $V_{2,4\ \mathrm{min}}$ and the maximum voltage value $V_{2,4\ \mathrm{max}}$ in 0.1 V steps. The measurement results for $V_{2,4\ \mathrm{min}}$=-3.5 V and $V_{2,4\ \mathrm{max}}$=3.5 V are shown in Fig. 2 (b). Initially, as $V_{2,4}$ decreased, $G_{1\text{-}3}$ increased to reach a high conductance state (HCS). Then, with increasing $V_{2,4}$, $G_{1\text{-}3}$ gradually decreased showing a plateau around 0 V, then further decreased and reached a low conductance state (LCS) at $V_{2,4\ \mathrm{max}}$. The LCS was maintained when $V_{2,4}$ was decreased again, forming a loop where $G_{1\text{-}3}$ exhibits HCS and LCS depending on $V_{2,4}$. We also observe gradual decrease of $G_{1\text{-}3}$ in HCS at $V_{2,4\ \mathrm{min}}$ when the $V_{2,4}$ voltage sweep is repeated, which was found to be related to the retention property of this device. The present results demonstrate the successful resistance switching operation of our four-terminal crossbar a-GaO_x memristor devices and the feasibility of integrated multi-terminal memristor array architectures.

Acknowledgments: This work was partially supported by a KAKENHI Grant-in-Aid (JP20H00248, JP23H01687, JP24K00926) from the Japan Society for the Promotion of Science (JSPS).

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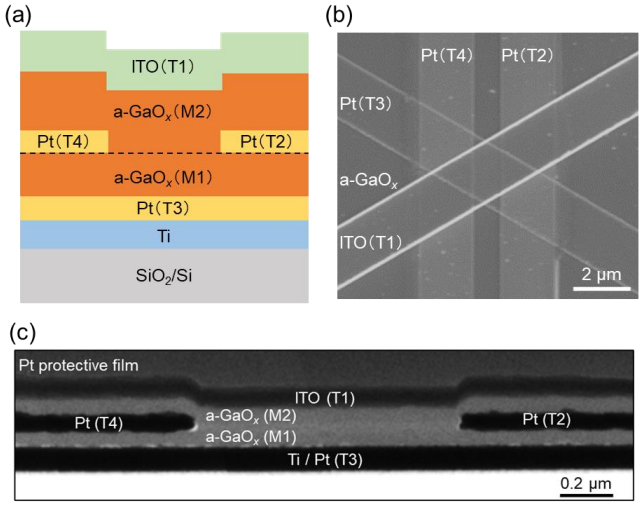

Figure 1. (a) Cross-sectional schematic and (b) plan-view SEM images of the fabricated device. (c) Cross-sectional TEM image of the four-terminal crosspoint of the fabricated device.

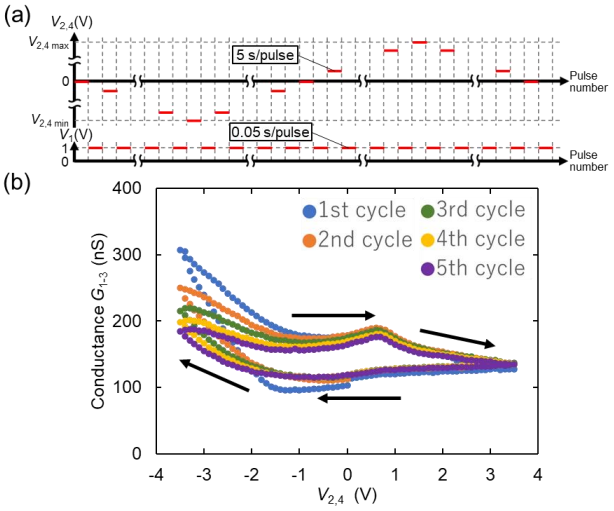

Figure 2. (a) Voltage application protocol of $V_{2,4}$ and V_1. (b) Variation of $G_{1\text{-}3}$ after respective steps of $V_{2,4}$ application. Blue, orange, green, yellow and purple curves show the first, second, third, fourth and fifth cycles of the $V_{2,4}$ applications, respectively.

Reconfigurable Devices for Enhanced Reservoir Computing

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Reservoir Computing (RC) is a machine-learning algorithm for processing time-series signals generated by complex dynamical systems, emulating the human brain's highly nonlinear and recursively interconnected architectures. It is a type of recurrent neural network that employs a "reservoir" as a dynamic feature extractor to process sequential or time series data. The reservoir layer is a vital component of the RC system, extracting features from the temporal input data. The main advantage of the RC is the minimal training data sets and an easy training process through a compact structure. Nonetheless, the conventional RC system has been primarily software-based, assuming its operation in the CMOS circuits. Such RC systems undermine their crucial merits due to extensive data use, which is the critical hurdle of the current von Neumann computing system[1].

This work investigates the potential of reconfigurable devices to enhance RC performance by generating diverse nonlinear dynamics within the reservoir (Figure 1a). Three distinct devices are adopted using their unique physical mechanisms that exhibit volatile nonlinear behaviors, demonstrating that integrating multiple reservoir units with varying dynamics significantly enhances overall RC performance. The first device is a $Pt/Ta_2O_5/HfO_2/TiN$ memristor, which leverages the electronic trapping properties of HfO_2 combined with either a self-rectifying or a resistive Ta_2O_5 layer (Figure 1b). The different microscopic configurations lead to distinct relaxation behaviors, thereby diversifying the reservoir dynamics. The second device is a $CuTe/HfO_2/Pt$ memristor, which employs a CuTe filament within a trapping device (Figure 1c). Its volatile behavior can be selectively turned on or off, altering its dynamic response based on the number of active devices within the reservoir. The last device is a two IGZO transistor structure (2T0C) working as a gain cell. By controlling the V_{GATE} of the write transistor, the nonlinearity in the current relaxation can be monotonically tuned, providing fine control over the reservoir dynamics (Figure 1d). Integrating reconfigurable units with diverse behaviors within the reservoir overcomes the limitations of previous hardware implementations and highlights a promising pathway toward more robust and efficient RC systems.

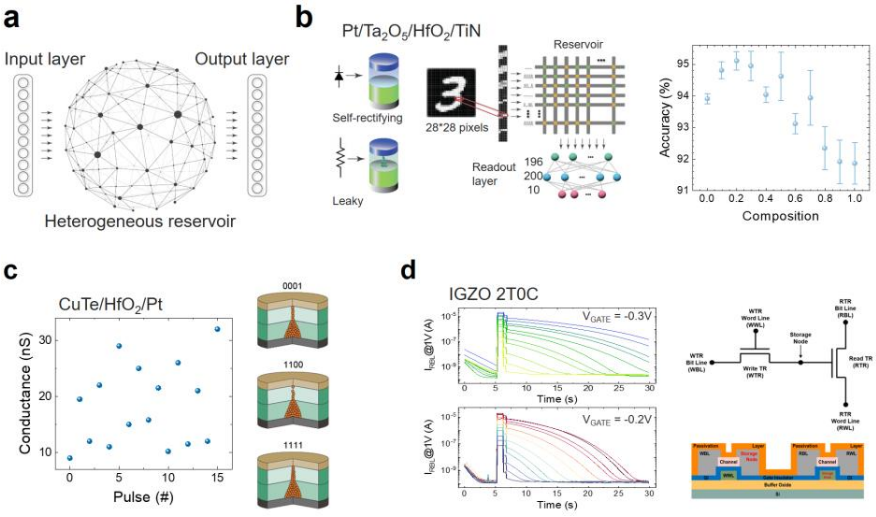

Figure 1. (a) Heterogeneous reservoir computing structure where the reservoir units present different dynamic response. (b) Reservoir composed of self-rectifying and leaky $Pt/Ta_2O_5/HfO_2/TiN$ memristor, resulting in a 5% performance increase. (c) $CuTe/HfO_2/Pt$ memristor based- reservoir presents a strong separability for 4-bit pulse pattern due to the different Cu filament morphology. (d) 2T0C gain cell device structure allows the fine control of the relaxation dynamics by means of V_{GATE}.

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Self-selective Crossbar Synapse Array with n-ZnO/p-NiO_x/n-ZnO Structure for Neuromorphic Computing

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Artificial synapse devices are essential elements for highly energy-efficient neuromorphic computing, which can overcome the current bottle neck issue of the von Neuman computing system[1,2]. They are implemented as crossbar array architecture, where highly selective synaptic weight update for training and sneak leakage-free inference operations are required. In this study, self-selective bipolar artificial synapse device was proposed with n-ZnO/p-NiO_x/n-ZnO heterojunction and its analog synapse operation with high selectivity was demonstrated in 32×32 crossbar array architecture without the aid of selector devices (**Figure 1** and **Figure 2**). The built-in potential barrier at p-NiO_x/n-ZnO junction and the additional current flow due to Zener tunneling effect provided nonlinear current-voltage characteristics at both voltage polarities for self-selecting function for synaptic potentiation and depression operations (**Figure 3**). Voltage-driven redistribution of oxygen ions inside n-p-n oxide structure, evidenced by x-ray photoelectron spectroscopy, modulated the distribution of oxygen vacancies in the layers and consequent conductance in an analog manner for synaptic weight update operation (**Figure 4**). It demonstrated that the proposed n-p-n oxide device is a promising artificial synapse device implementing self-selectivity and analog synaptic weight update in a crossbar array architecture for neuromorphic computing.

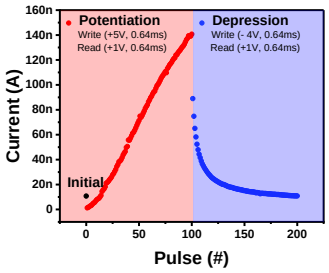

Figure 1. Synaptic analog conductance modulation behavior

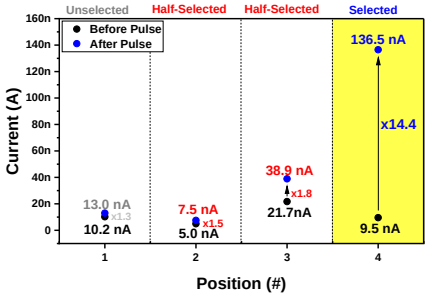

Figure 2. Highly selective conductance modulation in 32×32 crossbar array device

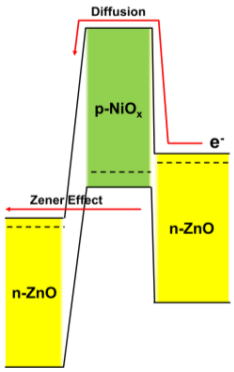

Figure 3. Nonlinear current-voltage characteristics due to built-in potential barrier and Zenner tunneling effect

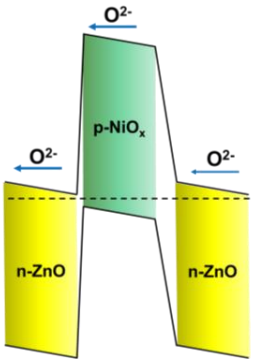

Figure 4. Change of energy band by voltage-driven redistribution of oxygen ions resulting analog conductance modulation

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An $ErMnO_3$ memristive spiking neuristor

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We present a novel $ErMnO_3$ memristive device exhibiting a negative differential resistance (NDR) region. By biasing this device in the NDR region and including a RC circuit, we have created a spiking neuristor capable of emulating the leaky-integrate-and-fire behavior of biological neurons, see Figures 1-3. The neuristor leverages the local activity phenomenon in the volatile memristive threshold switching device, enabling it to mimic the spike dynamics of natural neurons. Despite advances that have been achieved by utilizing NbO_2 and VO_2-based NDR devices, controlling their reliability and the spiking frequency range remains challenging due to their temperature-driven mechanisms. With a focus on this aspect, we developed a compact model, which describes accurately the experimentally measured behavior at room and elevated temperatures, and predicts the internal temperature during the neuristor operation. The model expands our previous research [1] and treats the internal temperature as the memristor state variable while assuming Poole-Frenkel emission [2] as the primary mechanism combined with an internal bipolar diode behavior. Following the strong agreement between DC experimental data and the proposed model, see Figure 2, we extracted analytically the element values of the small-signal equivalent circuit parameters, including the equivalent inductance in the locally active region.

In order to determine the most reliable operation across a wide frequency range, we explored different biasing schemes while carefully tuning the element values of the circuit depicted in Figure 1. We observed a consistent and reliable spike response with minimal jitter and noise throughout the experiments. The proposed model can accurately reproduce the same waveform response observed in the measurements, as shown in Figure 3. The spike interval frequency can be varied from 100 kHz to 300 kHz by adjusting the input source voltage or biasing regime. By utilizing our neuristor model, we designed a trade-off between resistive damping and limiting the internal temperature, ensuring safe operation and preventing unintentional non-volatile behavior by not exceeding the annealing temperature of the device. Finally, we simulated our model in SPICE and demonstrated a spike propagation along neuristor cells. This research aims to pave the way for low-power hardware implementations of spiking neural networks, capitalizing on their sparse and event-based operation paradigm to effectively conserve energy.

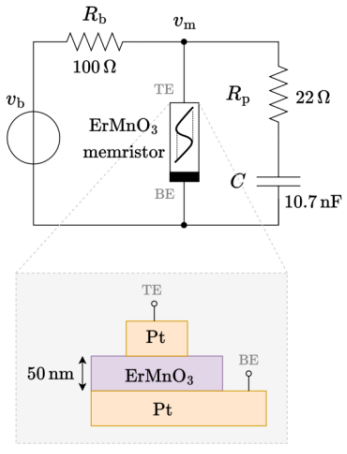

Figure 1. Neuristor circuit to bias the $ErMnO_3$ device in the NDR region. The device is connected via a probe station with the external biasing circuit.

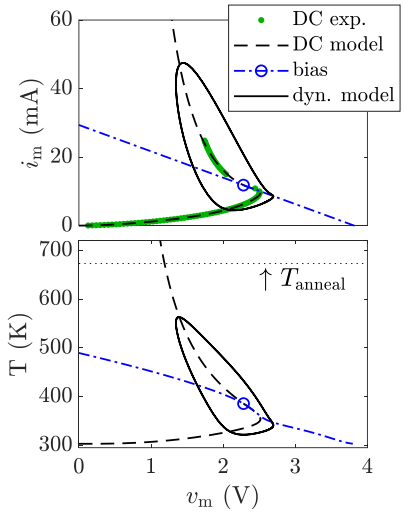

Figure 2. Static and dynamic phase diagrams: memristor current (upper) and internal temperature state (lower) versus memristor voltage. Experimental DC data (green dots) overlap with DC model (black dashed line).

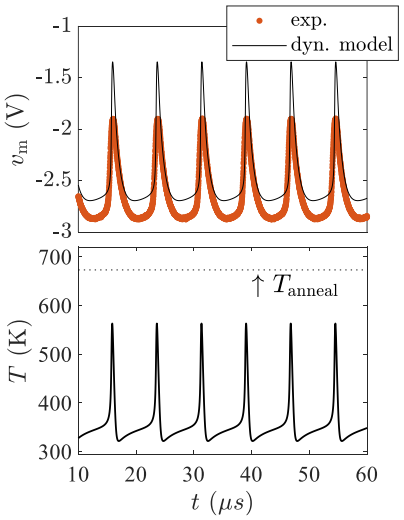

Figure 3. Time responses for memristor voltage (upper) and internal temperature state (lower). Experimental data (red dots) and dynamic model (black line) show same waveform at a spike frequency of 130 kHz.

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V-VTEAM: A Compact Behavioral Model for Volatile Memristors

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Volatile memristors have recently gained popularity as promising devices for neuromorphic circuits, capable of mimicking the leaky function of neurons and offering advantages over capacitor-based circuits in terms of power dissipation and area. Additionally, volatile memristors are useful as selector devices and for hardware security circuits such as physical unclonable functions. To facilitate the design and simulation of circuits, a compact behavioral model is essential. This paper proposes V-VTEAM, a compact, simple, general, and flexible behavioral model for volatile memristors, inspired by the VTEAM nonvolatile memristor model and developed in MATLAB. The validity of the model is demonstrated by fitting it to an ion drift/diffusion-based Ag/SiOx/C/W volatile memristor, achieving a relative root mean error square of 4.5%.

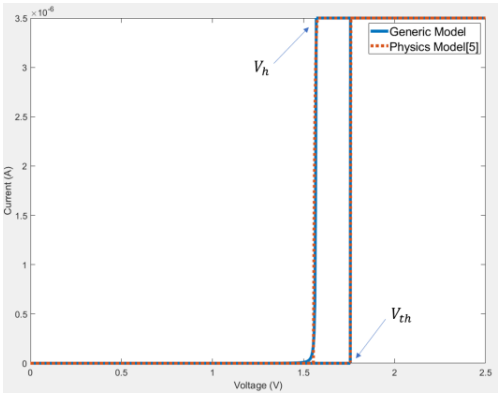

Figure 1. Proposed Generic Model fitted to an ion drift/diffusion-based Ag/SiOx/C/W volatile memristor model [5].

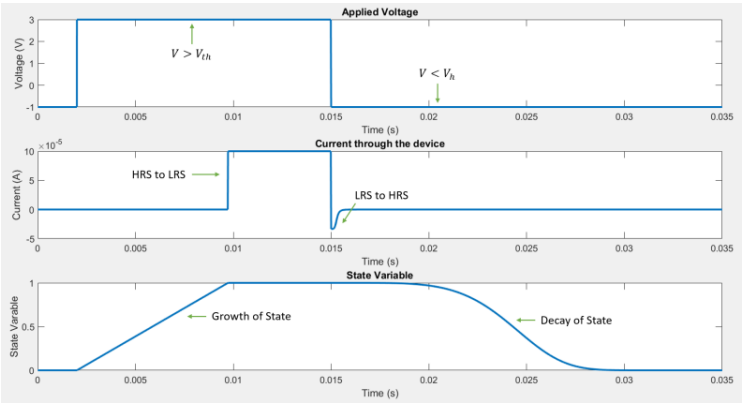

Figure 2. The applied voltage, current, and state variable of the proposed volatile memristor model

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Emergence of *In Materia* Intelligence in Energy-efficient Neuromorphic Devices realized using Self-forming Hierarchical Structures

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Emulating brain-like functions using electronic circuits has always been the holy grail for the scientific community for decades. For this purpose, already developed conventional computing architecture limited by von Neumann bottleneck consumes an enormous amount of energy while facing several other challenges.[1] Neuromorphic devices made of two-terminal resistive switching memristors such as valence change memory (VCM), electrochemical metallization (ECM) and others, operating on different mechanisms are promising due to the possibility of achieving high integration density and low power consumption.[2] Among all, the dynamic formation and relaxation of conductive metallic filaments in ECM devices under electrical pulsing is rather intricate and has much more to offer.[3] Although, the artificial synaptic devices in literature are paradigms of complex computing tasks but often lack the inherent dynamically evolving topology of the biological neural network (BNN), considered as the basis for various cognitive functionalities.[4,5] Closely mimicking the hierarchical structural topology with emerging behavioral functionalities of BNN in neuromorphic devices comprising a network of synapses is considered of prime importance for the realization of energy-efficient intelligent systems. In this regard, building an artificial synaptic network (ASN) using a self-forming approach seems promising due to structural similarity with the biological system and low fabrication cost.[6] We have developed an ASN comprising of hierarchical structures of isolated Al and Ag micro–nano structures developed via the utilization of a desiccated crack pattern, anisotropic dewetting, and self-formation.[7] The strategically designed ASN, despite having multiple synaptic junctions between electrodes, exhibits a threshold switching (V_{th} ~ 1–2 V) with an ultra-low energy requirement of ~1.3 fJ per synaptic event. The emerging potentiation behavior of the conductance (G) profile under electrical stimulation and its permanence beyond are realized over a wide current compliance range of 0.25 to 300 µA, broadly classifying the short- and long-term potentiation grounded on the characteristics of filamentary structures. The scale-free correlation of potentiation in the device hosting metallic filaments of diverse shapes and strengths evidence of *in materia* intelligence providing an ideal platform for understanding and replicating the complex behavior of the brain for neuromorphic computing.

Figure 1. Self-formed hierarchical structures of Al (blue) and Ag (grey) of different length scales (left side), closely mimic the structural hierarchy of biological neural network (right side). Diverse range of Ag filamentary structures (red) show wide ranging synaptic plasticity similar to biological counterpart.

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Multi-level switching in 1T1R memristive cells: A simulation approach by compact model

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Memristive device based on valence change mechanism (VCM) is one of the most attractive candidates for nano-scale memory electronics because of its fast write/read speed, excellent scalability, and low energy consumption [1,2]. Especially, due to its nonlinearity and multilevel behavior in electrical characteristics, memristive devices can take on an important role in neuromorphic computing applications to imitate an information processing system in human neural networks. The structure of the VCM memristive device cell consists of a simple metal/oxide/metal stack, with various types of oxide such as TaO_x, TiO_x, HfO_x, etc. [3,4]. To predict the electrical characteristics and the switching dynamics of VCMs on the device and circuit level, a simulation approach with a physically motivated compact model is needed. The switching process is induced by ionic migration and the conduction mechanism is figured out by analytical equations in the VCM compact model. The thermal resistance parameter in the compact model should be well-defined because thermal effects induced by Joule heating during switching can make a significant difference to electrical transfer by vacancy concentration change [5]. So far, the JART VCM v1b shows a constant thermal resistance during switching, which allows for a well-fitted behavior to binary switching devices, but the fitting of multilevel switching is less accurate.

In this study, we proposed the new JART VCM Rth compact model with state-dependent thermal resistance that allows for accurate modeling of multilevel programming. Previously, several compact models for VCM cells have been proposed [6], but in contrast to these previous versions, our JART VCM Rth compact model is now covering a change of the thermal resistance as a function of the oxygen vacancy concentration during switching. The compact model is applied to a 1T1R device for simulating multilevel switching controlled by different gate voltages applied to the serially connected transistor. The JART VCM Rth model allows for a much better fit to multilevel switching data than the JART VCM v1b model as shown in Fig. 1 and 2. The model also accounts for the device's inherent switching variability by variation of the filament geometry parameters [8].

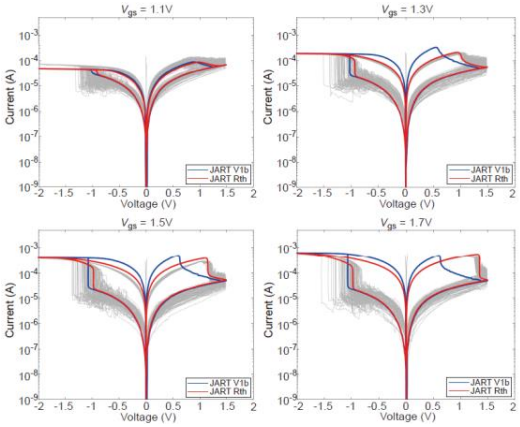

Figure 1. Simulated *I-V* sweep characteristics validated with 1T1R cell measurements

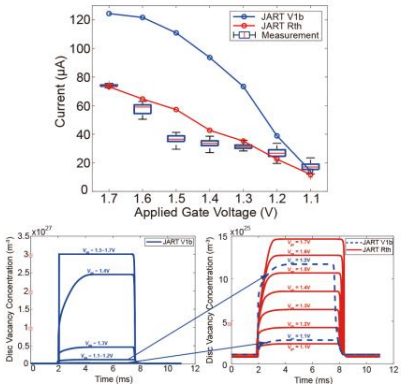

Figure 2. LRS current level after SET, and oxygen vacancy concentration during operation with multi-level switching

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Reservoir Computing for Pattern Recognition using Gd-doped CeO_2/CeO_2 Bi-layer Memristor

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Reservoir computing (RC) is a new powerful framework for effectively processing complex data, including pattern recognition, speech recognition, time series analysis, and natural language processing. While conventional feed-forward deep neural networks (DNNs) process signals by passing them from input to output, RCs are well suited for spatiotemporal signal processing by obtaining information from past inputs to influence current inputs and outputs. Unlike DNNs, requiring the entire weight network to be trained by the gradient method, RCs have an advantage in increased learning speed with reduced cost because training is performed only at the readout while maintaining the rest of the network fixed.

Among several device candidates for hardware implementation of RC systems, memristor is an proper and efficient device to apply to physical RC framework because it has nonlinear functions and exhibits memory characteristics [1]. Analyzing the time-dependent weight dynamics of memristors is important to extract various spatial and temporal characteristics of the reservoir in performing spatiotemporal operations in RC. These features include high dimensionality of reservoir, nonlinearity with respect to weight update, paired-pulse facilitation (PPF), short-term plasticity (STP), and class separation property. In particular, the reservoir state must have short-term decay characteristics to process spatiotemporal information via effectively separating complex sequential information without superimposing reservoir states. Therefore, it should be continuously pursued to investigate the time-dependent weight dynamics of memristors and improve those for their application to RC systems by achieving high-performance recognition and prediction in complex spatiotemporal tasks in RC systems.

In this work, we experimentally demonstrate an memristor-based RC system with Pt/Gd-doped CeO_2 (GDC)/CeO_2/Pt memristors exhibiting time-dependent weight update and decay characteristics, which benefit to realize RC systems. In this study, the bi-layered oxide memristors based on the same CeO_2 matrix, i.e., GDC/CeO_2, are employed, which are characterized to have by a more stable and controllable redistribution of oxygen vacancies between CeO_2 and GDC layers under the electric field. CeO_2 has high oxygen ion conductivity and variable valence states of Ce cations, which are favorable properties as a resistive switching material. GDC has also been reported to have increased oxygen ion conductivity via increased oxygen vacancy concentration as a result of Gd doping in CeO_2. The proposed GDC/CeO_2 bi-layered oxide memristor has been demonstrated to have analogous synaptic weight update, PPF, STP characteristics and their adjustment could be improved compared to the single-layered CeO_2 or GDC memristors [2]. Thus, this GDC/CeO_2 bi-layered memristors are expected to perform RC by storing reservoir states with controllable weight update and decay characteristics that effectively separate complex sequential information without superimposing the states. The RC performance of the memristor was evaluated by a 4-bit pattern verification as applying various pulse signals to the memristor using Modified National Institute of Standards and Technology (MNIST) handwriting database to train and test the RC system. Pattern recognition simulations showed accuracy levels of up to 90% in bilayer memristors, confirming the potential of these bilayer memristors as artificial synapses for neuromorphic computing.

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Low-Power and Thermally Stable Phase Change Memory by Material Engineering of Phase-Changeable Nano-Filament

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Conventional $Ge_2Sb_2Te_5$ (GST)-based phase change memory (PCM) has attracted attention as a next-generation non-volatile memory technology due to its simple two-terminal structure and high scalability. However, the high reset current of conventional PCMs deteriorates the energy efficiency of PCM-based applications [1]. Furthermore, the poor thermal stability of the GST, stemming from its low glass-transition temperature (T_g) of approximately 160 °C, limits its use in high-temperature applications [2]. Here, we developed a thermally stable and low-power PCM with high glass-transition temperature (~286 °C) and low RESET current (<100 μA) by forming an alloyed phase-changeable nano-filament. The narrow dimension of the alloyed filament enables a low RESET current regardless of the fabricated device size. Additionally, the alloying of Si in the phase-changeable filament increases the T_g of the filament, resulting in a good thermal stability. Based on the improved thermal stability and reduced power consumption, we expect that the developed device could be utilized for various applications in high-temperature and limited power environments, such as edge systems for automobiles, robots, or airplanes.

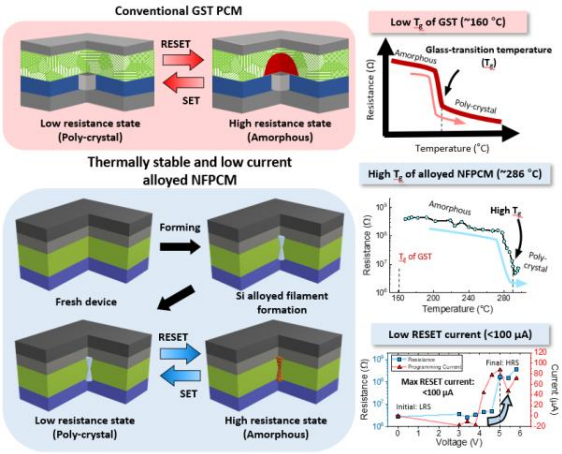

Figure 1. Schematics of the alloyed NFPCM compared to conventional GST-based PCM, and its high thermal stability and low RESET current characteristics [3]

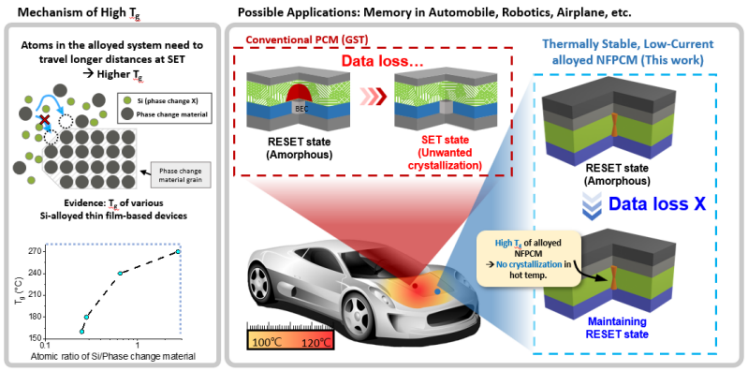

Figure 2. Mechanism of the high T_g of the alloyed NFPCM and its possible applications

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Fabrication of 4k Density Vertical Resistive Switching Memory for Neuromorphic Applications

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The advent of artificial intelligence and other data-intensive technologies has highlighted the limitations of traditional von Neumann architectures, particularly the time and energy costs associated with data movement. In-memory computing (IMC) architectures have been proposed to address these inefficiencies. One of the most promising hardware prototypes for IMC is resistive switching random access memory (RRAM), which provides non-volatile memory storage and has the potential to perform logic operations. Nevertheless, the sneak path problem in highly integrated and large-scale arrays poses a significant challenge[1]. A promising approach to mitigate these issues is the introduction of a three-dimensional vertical array with self-rectifying RRAM[2].

This work presents the fabrication and evaluation of a 4-layer vertical RRAM (V-RRAM) array comprising 32x32 Pt/Ta_2O_5/Al-doped HfO_2 /TiN (PTHT) memristor cells (Figure 1a). The array utilizes a shared top Pt electrode, while four distinct bottom TiN electrodes are deposited. Figure 1b displays a cross-sectional TEM image, clearly illustrating the correct stacking of the four devices in one array position. Electrical I-V sweeps were conducted using an 8x4 multi-probe system to measure the entire 4k V-RRAM array. Figure 1c shows typical electrical characteristics results of 1k devices for the 4th layer. Device-to-device and cycle-to-cycle characteristics were analyzed in detail, and statistical parameters for all layers were extracted.

The 4k V-RRAM array demonstrates a mean yield of approximately 85% across the four layers. The high yield is attributed to the deposition of Al-doped HfO_2 and Ta_2O_5 films by atomic layer deposition. However, layer 1 exhibits a lower performance than the other layers due to the non-uniformity of the etching process inside the etched hole. A steeper etching process is required to enhance the overall yield to a value exceeding 95%. Figure 1d compares the I-V responses for the four layers, revealing similar behavior across all layers. The multilayer structure and multi-functionality of the PTHT memristors enable parallel processing of diverse neuromorphic tasks within the same device, offering a pathway towards efficient and integrated neuromorphic computing systems.

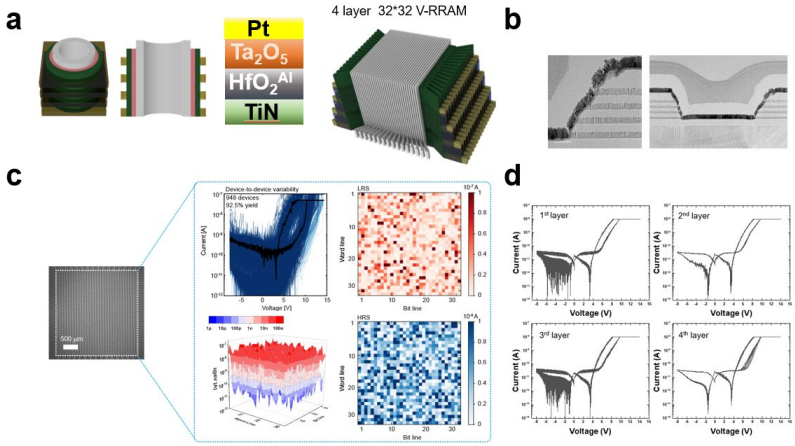

Figure 1. (a) 3D diagram of a 4-layer V-RRAM array comprising 32x32 Pt/Ta_2O_5/Al-doped HfO_2 /TiN (PTHT) (b) SEM image of a 4-layer device. (c) Typical electrical characteristics for the 1000 devices in 4th layer. (d) Comparison of the electrical behavior for the 4 layers, exhibiting qualitatively similar behavior.

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Low Power and Reliable Dynamic Memtransistor with Step-Wise Potential Barrier for Energy-Efficient Computing

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We are living in the era of artificial intelligence. Technological advancements are generating more data, and the artificial intelligence models to process it are becoming increasingly complex. However, modern computer architectures are inefficient, leading to wasteful use of resources. Given that our resources are finite, we need to find a more efficient computing framework.

In this study, we propose a low-power device applicable to neuromorphic computing for efficient computing. We have developed a 3-terminal memtransistor with a step-wise potential barrier (Figure 1). It consists of a channel, a charge storage layer (CSL), and a blocking layer (BL), with the conduction band of the CSL positioned below that of the channel. Electrons are stored in the CSL due to the step-wise potential, allowing for analog control of the channel's conductance based on the amount of charge stored in the CSL. Electron programming or erasing can be achieved through gate bias.

The primary advantage of the structure with a step-wise potential barrier lies in its fast operation. Since there is no effective barrier when electrons move from the channel to the CSL, conductance updates are possible even with very rapid voltage pulses. Moreover, at zero bias, the stored electrons gradually escape to the channel due to the low step-wise barrier, enabling the implementation of dynamic characteristics. Additionally, CMOS-compatible processes and the 3-terminal structure ensure high reliability and low-power operation (Figure 2).

We have implemented reservoir computing using dynamic memtransistors (Figure 3). By utilizing the dynamic characteristics that change over time, we can extract features from temporal data and store them in the channel conductance. We have confirmed that these stored features effectively retain the information of the original data.

Through this research, we have validated the potential use of dynamic memtransistors, which are highly reliable, high-speed, and low-power, for new algorithms.

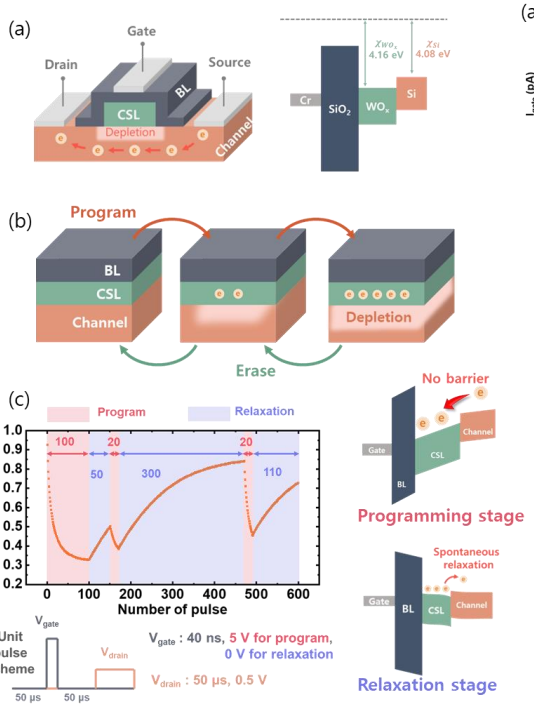

Figure 1. (a) 3-termimal, step-wise potential barrier structure, (b) analogue conductance update, and (c) dynamic characteristics

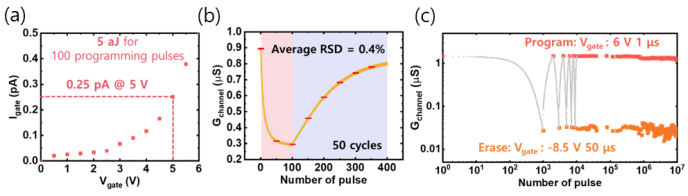

Figure 2 (a) Low power, (b) low variation, and (c) high endurance characteristics

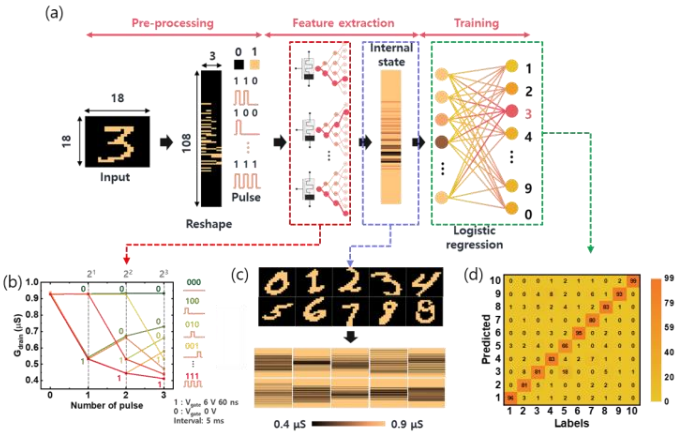

Figure 3 (a) Reservoir computing of MNIST classification simulation framework, (b) temporal feature extraction, (c) stored conductance, and (d) classification accuracy result

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A combined approach of numerical simulation and *ab initio* calculations on $Ag/HfO_2/RuO_2$ diffusive memristor for probabilistic computation application

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The memristor-based probabilistic bit (p-bit) emerges as a promising next-generation computing unit for probabilistic computing, adept at handling complex tasks involving big data. However, the origin of stochastic behavior inherent in the p-bit and the factors influencing this stochasticity remain unclear, hindering systematic studies on the p-bit. In this work, finite-element method (FEM) simulations of $Ag/HfO_2/RuO_2$ stacks, a representative memristor-based p-bit device, were conducted to analyze the intrinsic stochasticity observed in SET operation. The necessary physical parameters for the model are derived from *ab initio* calculations, enhancing the physical accuracy of the model. This model accurately reproduces experimental results and demonstrates that the primary source of the stochasticity originates from the randomness in the detachment time of Ag^+ ions from the electrode to the oxide. Furthermore, extrinsic factors affecting the stochasticity, such as operating voltage and temperature, were investigated, providing guidelines for controlling the stochasticity. These guidelines are validated through experimental feedback.

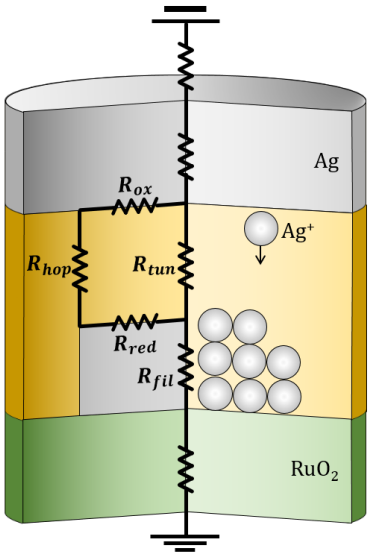

Figure 1. Schematic of p-bit model.

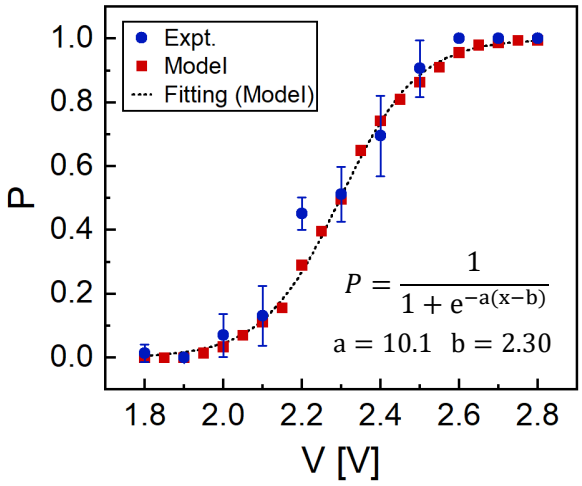

Figure 2. Sigmoid plot predicted by p-bit model

Long-Term Stability Testing of Memristors: Pulsed Read Endurance Measurements On Yttria-based OxRAM

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For a widespread adoption of memristive devices, long-term stability of their state is essential. This property is particularly important in the context of neuromorphic applications, where the state of a device must be stable not only for a binary LRS or HRS, but also for any number of intermediate states. Unfortunately, most memristive devices exhibit a drift of resistance, intensified or caused by the process of reading out their state. When used as a memory device, e.g. as a flash replacement, memristive devices are typically read out with short read pulses.

To evaluate long-term stability, we propose a measurement setup consisting of a readout pulse source, providing short ($\leq 10ns$) pulses at a low voltage ($175mV$), and a current-compliant source for applying write pulses ($\pm 3\ V, \pm 60\ mA, \geq 5\ ns$). This combination first allows the device to be set to the desired state. It is then possible to apply many billions of readout pulses while verifying every few pulses that the device's conductance has not drifted out of the desired range, finally moving on to the next cycle without removing the device from the experimental setup. To reflect real-world applications and check compliance with automotive standards, the setup can be actively heated to up to $150°C$, providing insights into the long-term stability at higher temperatures. This allows us to capture meaningful and reliable endurance data, fulfilling and exceeding recommended procedures in the literature [1], including the acquisition of high-bandwidth U/I curves.

Long-term measurements of Y_2O_3-based memristors demonstrate a wide and stable on/off ratio, with no drift observed during the first million readout pulses nor for the subsequent $11 * 10^{11}$ pulses and beyond.

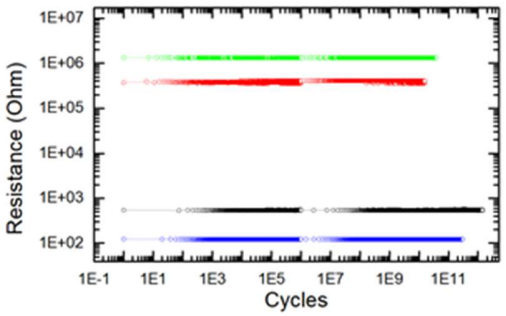

Figure 1. Decade measurement for a single Y_2O_3 device with one data point every decade for the first million pulses, then one measurement every 500 thousand pulses. Parameters: 175 mV and 100 MHz

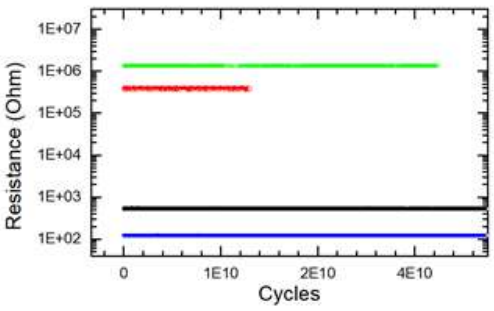

Figure 2. Endurance measurement, taken after every 10 thousand pulses. The test comprises of 100 MHz pulses with $175mV$ pulse amplitude. Linear cycle scale

References

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Thiazolothiazole Derivatives for Information Processing with Fine-Tuning Capabilities

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We present an innovative approach for fabricating high-performance, non-volatile memristors with the potential for use in flexible device forms. This was achieved by developing a group of novel materials capable of processing information upon electrical stimulation. Additionally, we designed and engineered device architectures that resulted in stable and instant (forming-less) memristive performance. The research includes the synthesis of thiazolothiazole derivatives, functionalized with various groups[1]. Figure 1 illustrates the exemplary structures of ortho-vanillin, cinnamic, and thiazole derivatives. Their role is to influence the metal-binding properties, charge carrier mobility, and photophysical characteristics of the compounds. Many of these materials are highly luminescent, and act as potential metal-binding sites. This is particularly intriguing, as the interactions with metal ions are not well understood, and their electrical properties, especially in memristive applications, remain largely unexplored.

Our studies suggest that Cu(II) complexes with thiazolothiazole-derived ligands are optimal for these applications. This selection is justified by their affinity to copper ions, which influences luminescent properties - enabling monitoring of device performance. Also electrical properties of pure thiazolothiazole-based ligands have been studied – see plots in Figure 1. Our findings demonstrate that various device architectures, when combined with appropriate materials and electronic measurement parameters, can indeed exhibit plasticity-like behaviors, making them suitable for neuromorphic computing.

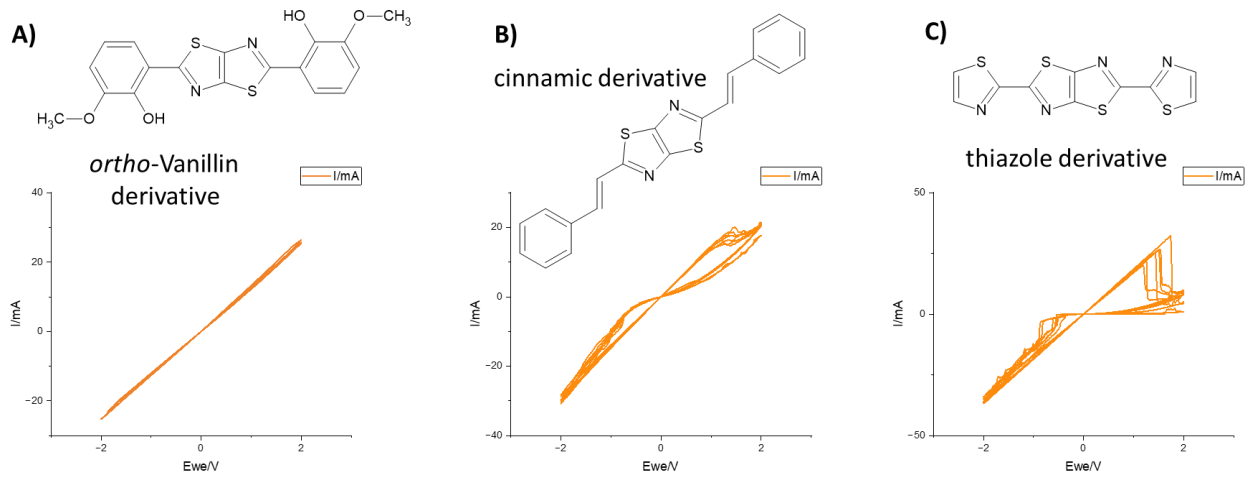

Figure 1. Chemical structures alongside with basic I-V responses of thiazolothiazole derivatives with numerous substituent groups: ortho-vanilin (A) cinnamic (B) and thiazole (C)

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Circuit-Based Modelling of Current Transients within the Memristive Devices Subthreshold Regime

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This study presents a model for a resistance switching device exhibiting current transients, where both analogue potentiation and conductance depression occur with the same voltage polarity, unlike previous devices. It explores the subthreshold region in memristors and resistance switching devices, characterized by current transients before switching [1]. Known as the subthreshold regime, this mode operates at biases insufficient for discrete or non-volatile switching. This behaviour potentially simplifies neural and synaptic circuitry in neuromorphic computing by eliminating the need for voltage pulses with opposing polarities. The work outlines methods to model and parameterize this behaviour using basic circuit components. These transients, featuring a distinct peaked response, have been utilized for various purposes, including estimating fault mobilities and implementing functions in neuromorphic circuits. An empirical SPICE model is provided to simulate these transients, validated with experimental data, with parameters supplied for readers to use in their simulations. The model improves on previous versions [2] by replacing voltage biases with diodes to better replicate Schottky-like contacts at metal-insulator interfaces and introducing relaxation dynamics observed when step potentials are removed, or the device is grounded.

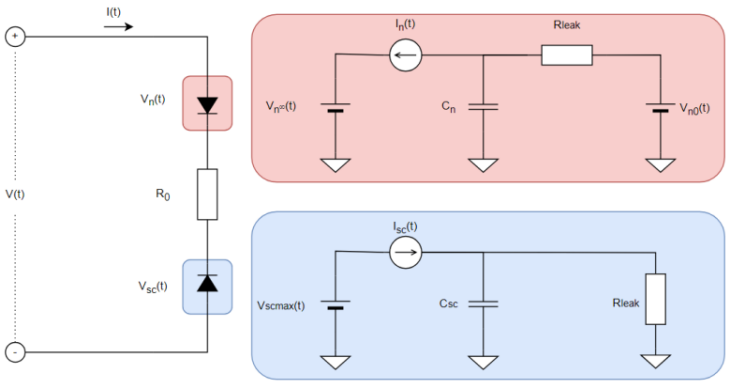

Figure 1. SPICE model diagram. The model produces an output current I(t), given an input voltage V(t). The circuit consists of a single resistor, R0, in addition to two diodes which act to reduce or increase the magnitude of the voltage applied to the resistor. resistor. These voltage sources are described by the sub-circuits highlighted in blue and red.

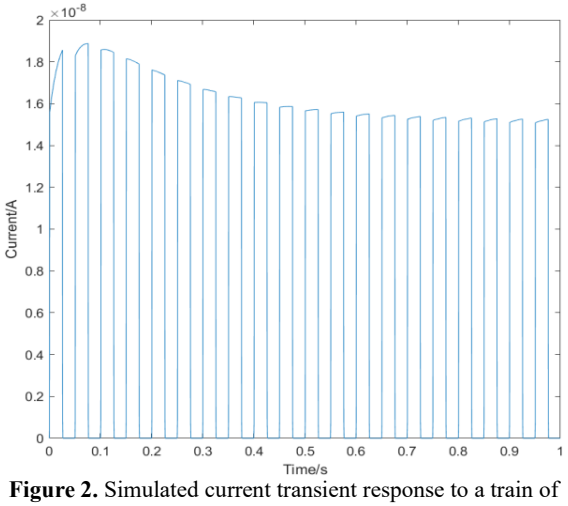

Figure 2. Simulated current transient response to a train of pulses. The current transients in amorphous silicon oxide devices appear to be the result of two separate changes occurring within the device simultaneously, resulting in both an increase and decrease in conductance.

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Design of the tri-valued memristor and its application

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In the field of digital logic circuits and nonlinear circuits, tri-valued memristors can simplify the circuit and enrich the circuit characteristics. In this paper, we propose an equivalent method of a tri-valued memristor which can be realized by using a commonly prepared binary memristor, and apply the tri-valued memristor obtained by this method to the design of ternary encoder, ternary decoder, ternary comparator and ternary data selector. The effectiveness of the circuit is verified by LTspice simulation.

Memristor-based Integrate-and-Fire with Homeostatic Plasticity for Simulation and Application

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This paper introduces a novel approach to emulating biological neural components using memristors, which are well-suited for this task due to their nanoscale size, resistance variability, and non-volatility. Inspired by the homeostatic switching behavior of biological neural components [1], illustrated in **Figure 1**, this study incorporates a homeostasis-based switching mechanism into the memristor model. The model is adaptable across various threshold-type memristor models and facilitates resistance adjustments in response to input signal changes, as depicted in **Figure 2**. A SPICE model of this memristor is developed to implement a neuron circuit that adheres to the homeostatic mechanism. Our proposed memristor-based integrate-and-fire neuron model with homeostatic plasticity supports two voltage levels in neural signaling: the spike peak and the rest potential [2]. The circuit schematic of this model is shown in **Figure 3**, highlighting its capability for homeostatic plasticity. Furthermore, a spiking neural network based on this model and its verification platform are designed, capable of performing pattern recognition. Simulations are conducted in Cadence PSPICE, comparing homeostatic and non-homeostatic scenarios to underscore the model's effectiveness, which shown in **Figure 4**. This work underscores the potential of memristors in advancing neuromorphic computing systems.

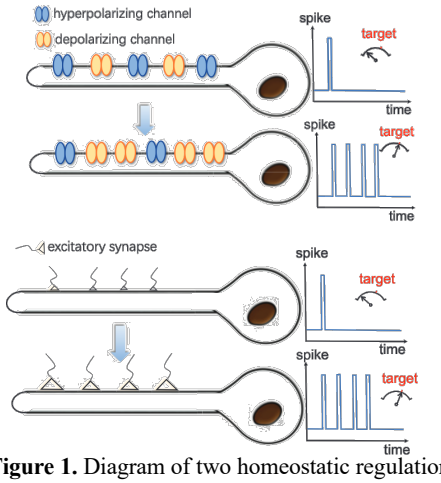

Figure 1. Diagram of two homeostatic regulations

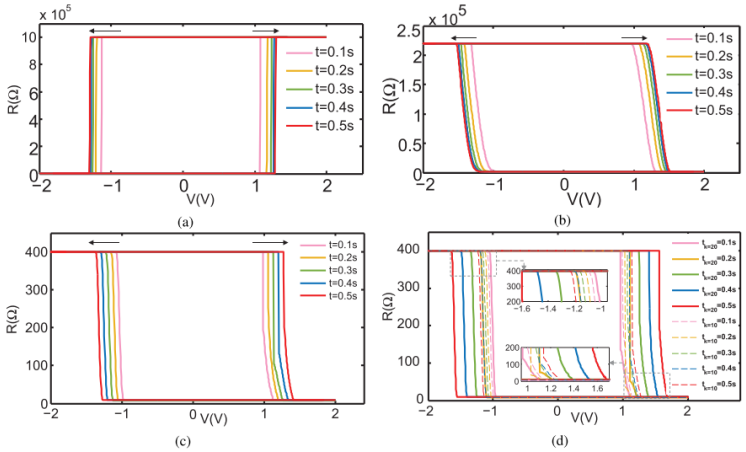

Figure 2. Numerical simulation results on different types of memristors

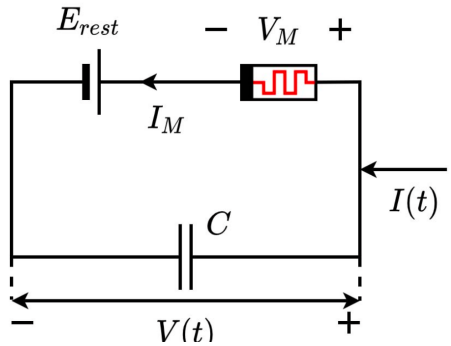

Figure 3. Diagram of two homeostatic regulations

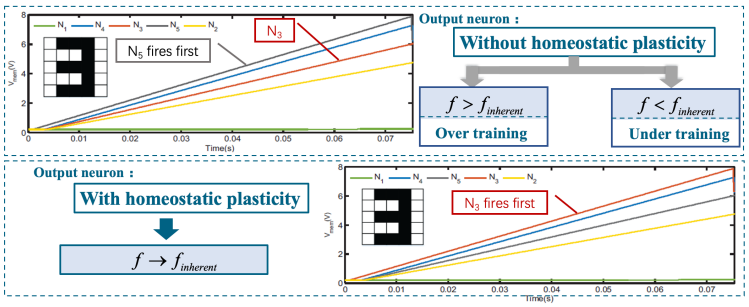

Figure 4. Parten recognition application based on the proposed spiking neural network

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Memimpedance-based Neural Adaptation Circuit with Hybrid CMOS/Volatile Memristor LIF Neuron

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Neural adaptation, allowing neurons to dynamically adjust their responses based on stimuli, significantly contributes to predictive coding, enhancing environmental selectivity, and maintaining neural systems at the edge of chaos [1], etc. The implementation of neural adaptation has aroused wide interest [2]; however, efficient implementation in hardware remains a challenge. In this paper, we propose a novel hardware implementation of neural adaptation based on hybrid CMOS/volatile memristor Leaky Integrate-and-Fire (LIF) Neuron Model, utilizing the observed memimpedance effect of memristors.

In Fig.1, we performed characterization for the memimpedance effect of our in-house fabricated HfOx-based memristors, using Keithley 4200A to realize specialized characterization pattern. The characterization flow includes two phases: 1. Applying multiple identical programming pulses to drive the memristor to different resistive state (RS). 2. Subsequently, applying a small AC signal of 0.5V, sweeping the frequency from 1kHz to 10MHz. RS is defined as the resistance under read pulses of 0.5V, preventing the device from switching. The cycle formed by the two phases is applied repeatedly, sweeping the voltage of the programming pulses in the first phase from 0.5V, 1V, 1.5V, ..., 6V, -0.5V, -1V, -1.5V, ..., -6V. The characterization results in Fig.1 are similar to the observation [3], where we can observe a clear positive correlation between RS and the capacitance in the memimpedance. In Fig. 2(a), the pulse source of the LIF neuron represents the input current received by the presynaptic membrane, while the Vout corresponds to the neuron spikes generated at the postsynaptic membrane. The current pulses integrated in the capacitor cause the Vout exceed the Vth of SnOx-based memristor, leading to the abruptly decrease in its RS and the Vout, forming a whole spike, as shown in Fig. 2(b). The spike is then propagating to the subsequent neuron. To realize neural adaptation, we replace the capacitor for integration in the LIF neuron with the HfOx-based memristor, to utilize the characterized memimpedance features for the integration with a time-varying integral coefficient (Capacitance). It allows the membrane Vth gradually to increase, leading to a progressively shorter output spikes until saturation. In Fig. 3, the simulation results in Cadence that is resemble to the biology neural adaptation [1] indicates the firing intensity descend with prolonged and repetitive stimuli.

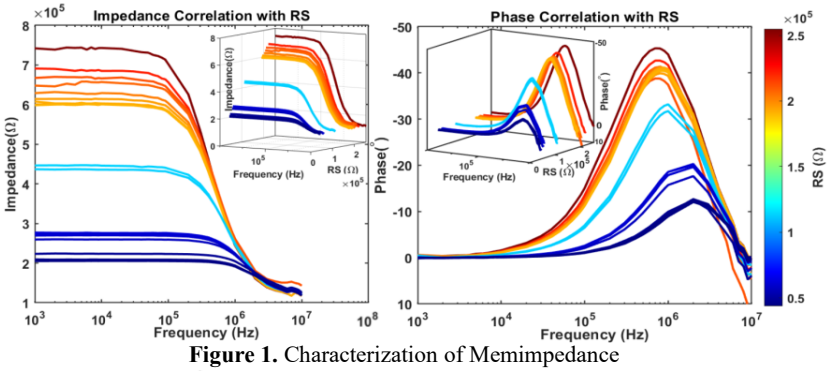

Figure 1. Characterization of Memimpedance

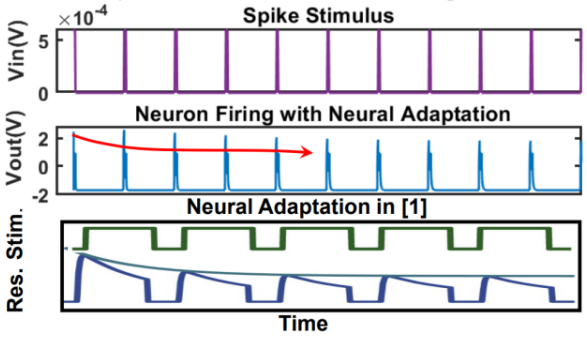

Figure 3. Simulation Results of Neural Adaptation

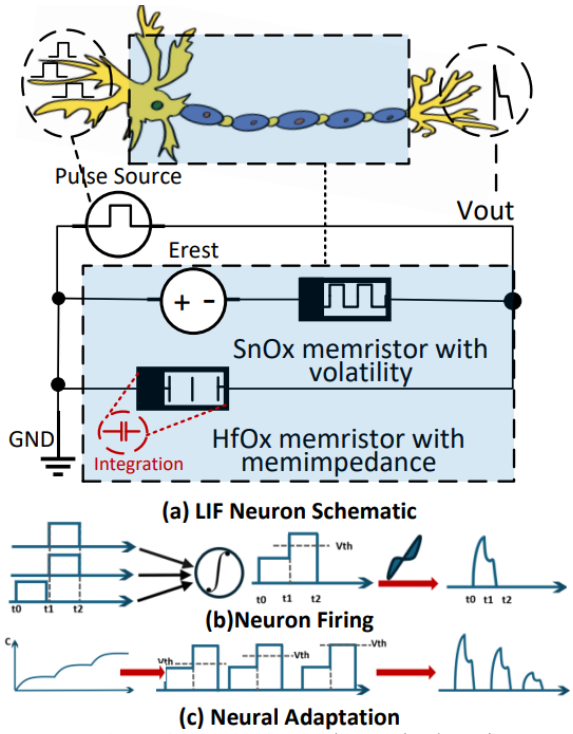

Figure 2. LIF Neuron and Neural Adaptation

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[2] Ganguly, C. et al., *Commun. Eng.*, 3(1), 22, 2024.
[3] S. Yu et al., IEEE Int. Electron Devices Meet., 12.1.1-12.1.4, 2011.

Effects of Surface Defect States on Memristive Switching in InP/ZnSe/ZnS Quantum Dot-based Memristors

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Memristors offer a promising solution to overcome the limitations of the von Neumann architecture by enabling efficient data storage and processing within a single device. Various materials have been explored for memristor applications, including metal oxides, two-dimensional materials, polymers, phase-change materials and quantum dots (QDs). Among these, QDs are particularly advantageous due to their tunable electronic properties, high areal density, and the ability to process both electrical and optical signals, making them highly suitable for memristor devices. In this study, we investigate the effects of surface defect states on the memristive switching mechanism of InP/ZnSe/ZnS QD memristors[1]. We design three distinct device configurations using a thin poly(methyl methacrylate) layer to identify whether electrons or holes are the primary charge carriers within the QDs layer. Through comprehensive analyses, we determine that electrons are predominantly trapped at the surface defect states, which are formed by zinc non-bonding states, of the InP/ZnSe/ZnS QDs, leading to memristive switching. Furthermore, we conducted numerical simulations using a TCAD device simulator to validate the charge trapping-based memristive switching in the InP/ZnSe/ZnS QD memristors, confirming that the memristive switching mechanism is governed by electron trapping in the surface defect states of the outer ZnS shell.

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Effect of molecular alignment on off current and switching properties in PEDOT:PSS-based RRAM

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Recently, resistive random access memory (RRAM) has emerged as one of the promising data storage devices, which has potential for next-generation technologies, such as neuromorphic computing, autonomous driving, and wearable devices. Especially, the use of organic materials as the active layer in RRAM offers significant advantages, including low-cost integration, environmental friendliness, and transient functionalities. Among several candidates, poly(3, 4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) stands out due to its highly tunable properties, such as molecular alignment, through simple treatments. Thus, it can be easily modified to optimize switching properties and performance metrics of RRAM, in accordance with the specific objectives. However, progress in leveraging the inherent properties of PEDOT:PSS in vertically stacked RRAM has been hindered by the limited research on the effects of its molecular alignment in the out-of-plane direction. Here, we propose two methods to modulate the molecular alignment in PEDOT:PSS, and verify that these methods impact the off current and data storage type in RRAM, respectively. First, we confirmed that a simple blending method using solid dopant molecules effectively reduced the off current, from 5.38×10^{-6} A to 3.20×10^{-8} A at a read voltage of 100 mV. It induced microstructural alignment of PSS without any removal, thereby serving as a blocking layer. In addition, we found that post-treatment of PEDOT:PSS film with organic solvent ordered the packing of the PEDOT chain with removal of PSS, which modified the switching property from nonvolatile to volatile. We believe that these two strategies present considerable potential for PEDOT:PSS-based RRAM to be used as low-power-operated neuromorphic devices with dual properties (i.e., nonvolatile and volatile), enabling both neural network functionality and short-term plasticity in neuromorphic applications.

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Energy-Efficient Capacitive-RRAM Dually Addressable Read Memory Core

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Access to memory acts as a major bottleneck for efficient computing within large systems, such as databases. This is evidenced by work to optimise memory storage such as [1,2], which seek to engineer ever better fundamental memory storage cells. In this work, we present an array-level dually-addressable memory module [3] that supports both content addressing and address addressing (Figure 1) using our home-fabricated RRAM in combination with commercially available 0.18um CMOS technology. Content-addressable reads (CAR) access memory with a search cue and output the addresses where the stored data matches the cue. The memory core can detect 64 sets of 64-bit data in parallel. On the contrary, address-addressable read (AAR) operates like traditional RAM, reading the data stored at a specified address. The system's digital controller operates at up to 875MHz clock (post-P&R simulation) and both read modes take 3x clock cycles to complete. The worst average energy is reported at 1.71fJ/bit-search for a CAR hit and 4.69fJ/bit-search for a CAR miss. The proposed energy-efficient solution reduces energy consumption and costs for data centres that are power-hungry with fast data processing.

The proposed bitcell (Figure 2) consists of 3-transistors, 1-RRAM and 1-capacitor C_b. The RRAM parasitic capacitance C_{mr} forms a capacitive divider with the physical capacitor. During content-addressable read (Figure 3) the search cue is presented at "cue" and "$\overline{cue}$", defining the content that the memory is looking for. The voltage at "mid" reaches different equilibrium voltages depending on the RRAM's resistive state. This voltage is further reflected on the match-line "ml" where V=high indicates data match (hit). The ternary state 'don't care' is also supported by setting both cue/$\overline{cue}$ to GND. During address-addressable read (Figure 4) charge from "cue" passes or doesn't pass on to the line capacitance of "psw" (depending on RRAM state), which acts as a charge tank. The charge level at psw is compared against a reference by a latch comparator, ultimately outputting AAR_out (Figure 5). Both CAR and AAR operations are charge-limited (no DC paths at any point). Only during (bidirectional) programming is the path "cue-RRAM-Q1-$\overline{cue}$" operated in DC mode. The fabricated chip (Figure 6) has a dimension of 1109um x 1163um.

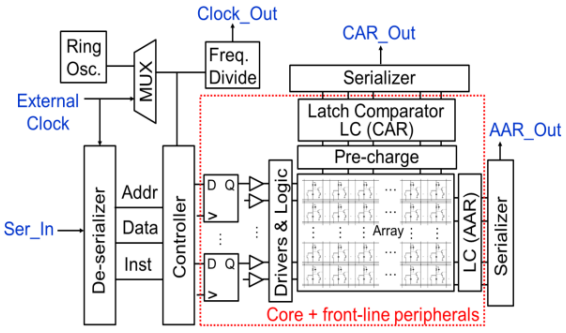

Figure 1. System Block Diagram.

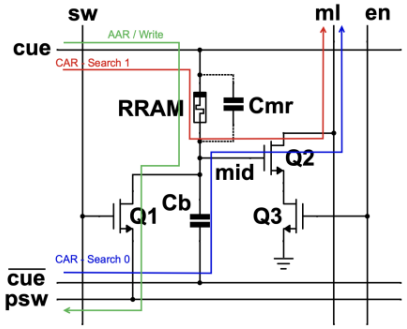

Figure 2. The 3T1R1C Bitell Schematic.

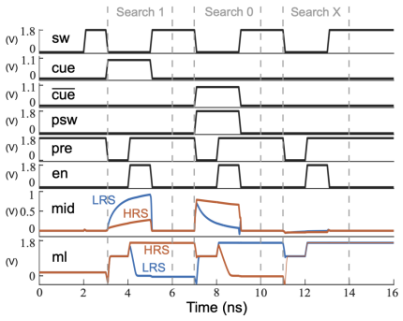

Figure 3. CAR Operation.

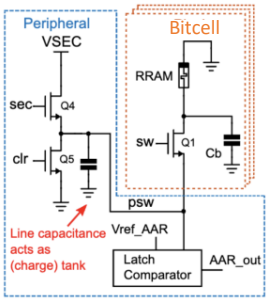

Figure 4. AAR Equivalent Schematic.

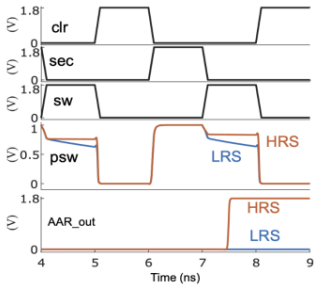

Figure 5. AAR Operation.

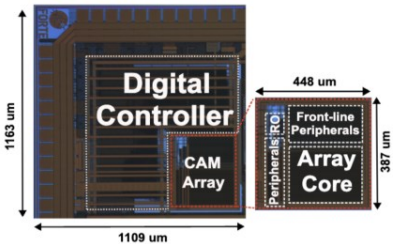

Figure 6. Fabricated Chip.

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Synaptic Behavior Implementation in a Highly Uniform Self-Rectifying Interfacial Memristor

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The emergence of artificial intelligence and big data has led to exponential growth in the amount of stored and processed data. Conventional von Neumann architecture has encountered several limitations in processing this huge amount of data. Therefore, neuromorphic computing, which emulates the operational behavior of the biological brain, has been proposed. Among many devices including emerging memories, a memristor has been widely studied to construct neuromorphic hardware, since it offers advantages such as a simple fabrication process and analog memory characteristics.

Previously reported interfacial memristors exhibited highly uniform and self-rectifying properties with an oxygen concentration gradient switching layer [1]. The oxygen gradient layer is fabricated by the oxidation of a thin metal film. Leveraging these properties, the device demonstrated potential in implementing artificial leaky-integrate-and-fire neuron models and sequential data processing. However, the device has some limitations in terms of demonstrating synaptic behaviors since the device exhibits fast decaying characteristics due to the spontaneous diffusion of oxygen anions. To successfully construct neuromorphic hardware, the implementation of synaptic functionalities is crucial.

In this study, we demonstrated the implementation of synaptic behavior in a highly uniform and self-rectifying interfacial memristor by adding an oxygen trap layer or an ion diffusion retarder (Figure 1). In a device with an oxygen trap layer, it exhibited low temporal and spatial variations (2.91% and 3.13%, respectively). Similarly, the device also exhibited low temporal and spatial variations (1.82% and 1.48%, respectively) and a high rectifying ratio (current ratio at V_{read} and $-V_{read}$) larger than 10^4 in a device with an ion diffusion retarder (Figure 2). Due to its high rectifying ratio, it possesses a significant advantage when implementing the memristor into a large crossbar array since it does not require additional elements such as transistors or selector devices. Furthermore, the results show that the device with an oxygen trap layer can represent the learning behavior of the biological brain through repeated stimuli. The device exhibited synaptic functionality such as short-term potentiation (STP) to long-term potentiation (LTP) under the consecutive pulse condition. Moreover, the multi-level representation was demonstrated by varying the stop voltage or the read voltage in a device with an ion diffusion retarder (Figure 3).

Through this research, we have developed a simple and effective way to implement synaptic behavior in a fast-decaying interfacial memristor, while maintaining highly uniform and self-rectifying properties.

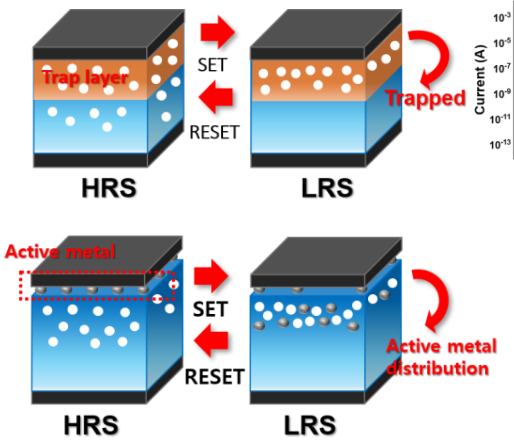

Figure 1. Schematics of an oxygen trap layer added device and an ion diffusion retarder added device

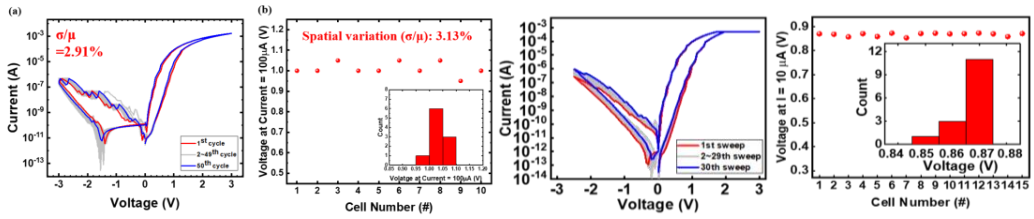

Figure 2. Temporal and spatial variation of the trap layer added device (left) and an ion diffusion retarder added device (right)

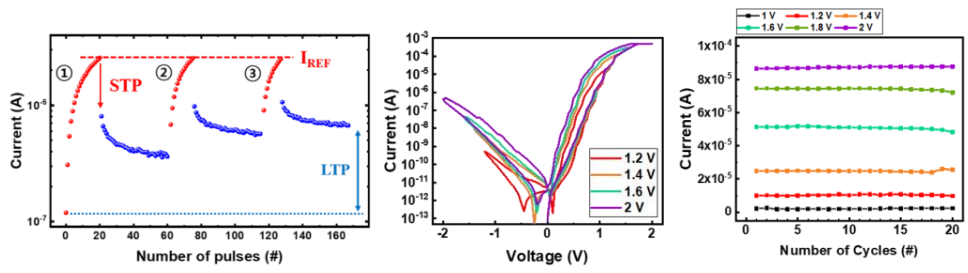

Figure 3. Learning behavior of the trap layer added device (left) and a demonstration of multi-level representation in a device with an ion diffusion retarder (center, right)

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Volatile and Nonvolatile Resistive Switching in Wafer-Scale MoS_2-based Memristors

Yuan Fa[1,2,*], Dennis Braun[2], Jimin Lee[2], Sofia Cruces[2], Lukas Völkel[2], Holger Lerch[1], Thorsten Wahlbrink[1], Jens Bolten[1], Annika Grundmann[2], Holger Kalisch[2], Michael Heuken[2,3], Andrei Vescan[2], and Max C. Lemme[1,2]

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Introduction: MoS_2, a two-dimensional material, has attracted enormous attention for neuromorphic computing applications due to its capability of resistive switching[1-5]. However, MoS_2-based memristors still suffer challenges of large cycle-to-cycle (c-c) variability due to intrinsic physical properties and defects introduced during material growth[2]. In addition, the future commercial exploration of MoS_2-based memristors requires scalable fabrication. Here, we present the wafer-scale integration of memristors with high-quality metal-organic chemical vapor deposited (MOCVD) MoS_2 with Ag and Pd electrodes, performing stable volatile and nonvolatile resistive switching (VS and NVS). Our memristors show low variability and stable state retention of at least 10^6 s, showing promise for large-scale usage of MOCVD MoS_2 memristors for neuromorphic computing.

Fabrication: MoS_2 memristors were fabricated on a 150 mm SiO_2/Si wafer (Fig. 1a). The Pd back electrodes (BE) and Ag top electrodes (TE) were defined by electron beam evaporation and a lift-off process (device schematic in Fig. 1b). MoS_2 was wet-transferred and patterned by CF_4/O_2 reactive ion etching. Fig. 1c shows Raman spectra of MoS_2 with identical peak positions before and after wet transfer. An MoS_2 thickness of 4.27 nm was measured by atomic force microscopy (AFM).

Results: We conducted current-voltage (*I-V*) measurements on memristors with an active area of 4×4 µm^2. 30 VS cycles were measured at each current compliance (I_{cc}) of 2.5 µA, 5 µA and 7.5 µA (Fig. 2a). We then increased I_{cc} and applied bipolar *I-V* sweeps, showing 35 and 100 cycles of forming-free NVS at 100 µA and 1 mA (Fig. 2b). At an I_{cc} of 100 µA, NVS happened between the initial high resistive state (HRS, ~10 MΩ) and a first low resistive state (LRS, ~3 kΩ), while at 1 mA, NVS happened between the first LRS and a second LRS (~300 Ω). The cumulative distribution functions (CDF) in Fig. 2c summarize the statistics of threshold voltages (V_t, VS), set voltages (V_{set}, NVS), and reset voltages (V_{reset}, NVS), showing low c-c variability. Fig. 2d shows stable retention of the three NVS states for over 10^6 s (V_{read} = 5 mV). Based on the VS and NVS, we hypothesize that the RS originates from Ag^+ ion migration from the TE[3–5], and filaments form and strengthen with increasing I_{cc}, eventually functioning as pseudo BE[5] during NVS between the first and second LRS. This memristor exhibits long-term potentiation during 80 consecutive voltage pulses (Fig. 2e), suggesting the formation of stronger filaments capable of resisting transient ruptures[6-7]. Our wafer-scale MoS_2-based memristors enable NVS and VS and show low c-c variability and stable retention, demonstrating the potential for neuromorphic computing.

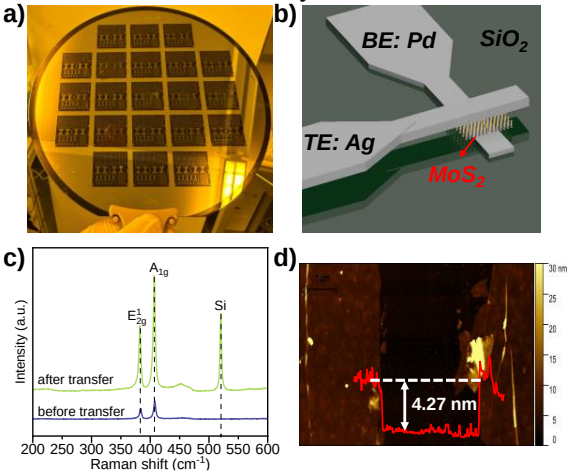

Figure 1. (a) Optical image of MoS_2 memristors on a 150 mm wafer. (b) Schematic of Ag/MoS_2/Pd memristors. (c) Raman spectra of MoS_2. (d) AFM image of as-grown MOCVD MoS_2.

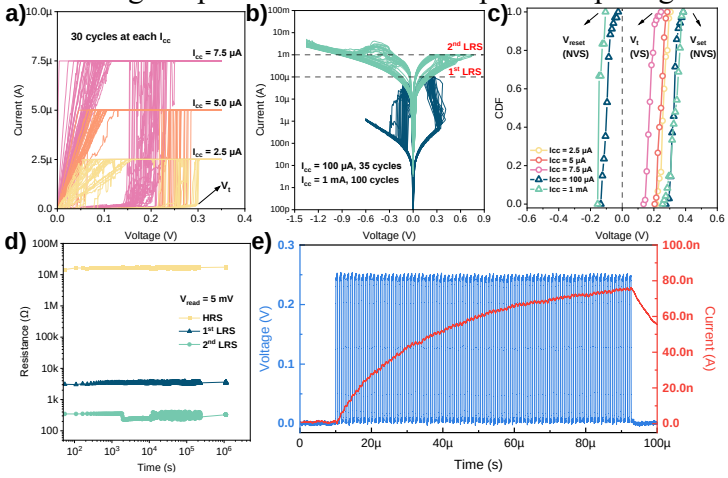

Figure 2. (a) 30 unipolar *I-V* curves at 3 different I_{cc}. (b) 35 and 100 bipolar *I-V* curves at I_{cc} of 100 µA and 1 mA. (b) CDF of data in (a-b). (d) State retention at 3 resistive states. (e) Current responses under 80 pulses.

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Analysis of 3-Dimensional Gate-Injection Field Effect Transistor with VNAND Structure for Area-Efficient Neuromorphic Hardware

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With the rapid advancement of artificial intelligence (AI), there is a growing need for new devices and computing methods that can manage large amounts of information. Neuromorphic computing has emerged as a promising candidate, providing efficient information processing and eliminating the bottleneck typically found between conventional processors and memory in the von Neumann architecture.

In the previous work, the gate-injection field effect transistor (GIFET) was researched to make the advantage of its high linearity as a synaptic device [1]. However, the necessity for high-capacity memory has become important, GIFET needs a new area-efficient structure. In recent years, VNAND has emerged as the area-efficient structure in flash memory technology.

In this research, we utilized the VNAND structure to fabricate a 2-layer Vertical GIFET (V-GIFET) and performed TCAD simulations to model a 10-layer V-GIFET. We achieved high linearity and low energy consumption during weight update. During the conductance update of the target cell, the inhibited cell exhibited 4.92% change in conductance compared to the target cell. Additionally, TCAD simulations confirmed that less than 10% of electrons migrated to adjacent cells when neighboring cells were programmed. This experimental data and simulation result indicate the feasibility of the V-GIFET as a vertical memory.

From this research, we have demonstrated the potential of the V-GIFET to serve as an area-efficient synaptic device in neuromorphic computing.

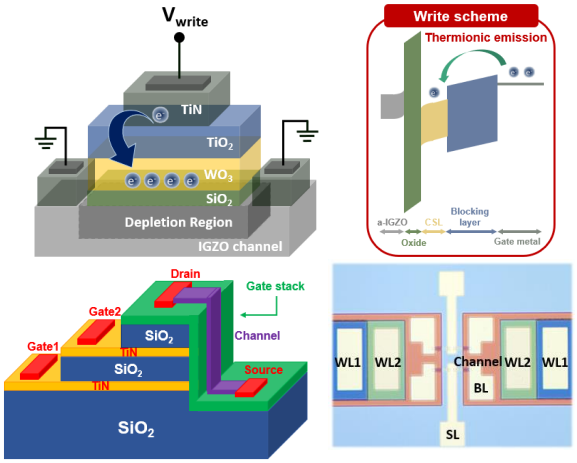

Figure 1. Scheme of the planar GIFET and writing scheme of GIFET (top), scheme of the V-GIFET and optical microscope image of the V-GIFET (bottom)

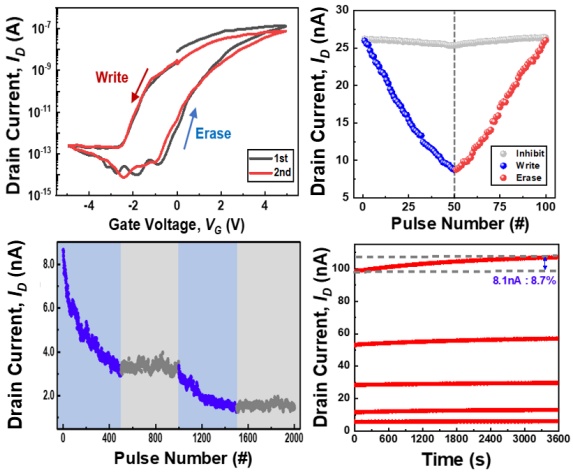

Figure 2. Electrical characteristics of the V-GIFET DC curve (top-left), LTD-LTP (top-right), retention characteristics (bottom)

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